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ABSTRACT

This study guide is part of an interdisciplinary curriculum entitled the Science and Engineering Technician (SET) Curriculum devised to provide basic information to train technicians in the use of electronic instruments and their application. The program of study integrates elements from the disciplines of chemistry, physics, mathematics, mechanical technology, electronics technology and electronics. The following topics are included in this guide: (1) diodes; (2) transistors; (3) regulated power supplies; (4) oscillators; (5) filter circuits; (6) digital concepts; (7) digital electronic circuits; (8) combinational logic; and (9) binary arithmetic. (Author/SK)

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This study guide is part of an interdisciplinary curriculum entitled the Science and Engineering Technician Curriculum (SET). The program of study integrates elements from the disciplines of chemistry, physics, mathematics, mechanical technology, and electronics technology, and electronics.

The purpose of this study guide is to provide basic information on electronic semiconductor devices and their applications. The following topics are included: (1) diodes, (2) transistors, (3) regulated power supplies, (4) oscillators, (5) filter circuits, (6) digital concepts, (7) digital electronic circuits, (8) combinational logic, and (10) binary arithmetic.

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Introduction

The purpose of this study guide is to provide a background of basic information on electronic semiconductor devices and their applications. The rapid growth of semiconductor technology is forcing changes in our approach to teaching and learning practical applications of electronic devices. Integrated circuit technology has now reached the stage where most commonly used circuits can be placed on a single I.C., even though they require thousands of electronic componenets. Circuit design theory is being replaced by circuit application and system design considerations because circuit design is already incorporated in the I.C.'s. Students must now become familiar with transfer characteristics of I.C. devices so as to understand how to inter-connect them and interface them with transducers to form operational systems.

Integrated circuits are divided into two broad categories: linear circuits and digital circuits. Linear circuits are used to process analog information in which the integrity of a continuously changing signal must be preserved. Digital circuits are used to process quantized information which is presented as a series of pulses.

Many of the functions formerly performed by dedicated logic gate circuits are now being performed by microprocessors which can be programmed to perform a wide range of logical operations. To provide an understanding of the language of microprocessors, a section on binary arithmetic and binary codes is also included in the digital circuit discussions.

Material in this study guide will provide the background needed to interpret the essential specifications and operational characteristics of basic analog and digital circuits.

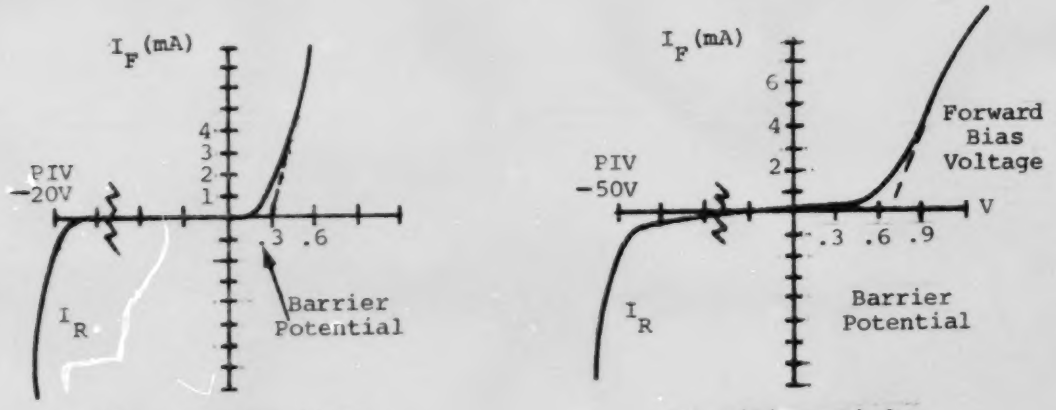
Section A - Diodes - Definition

Diodes are circuit elements which conduct electricity more readily in one direction than in the other. When N-type and P-type semiconductor materials are joined together, they form a junction diode which conducts when the P material is connected to a positive voltage and the N material is connected to a negative voltage (forward bias). When the polarity is reversed (reverse bias), the diode forms a high resistance.

At the junction of the N-type and P-type semiconductor material an exchange of electrons and holes across the junction forms a narrow region in which there are few holes in the P material and few electrons in the N material.

This is referred to as the depletion region. The opposite charge that builds up on each side of the junction creates a difference in potential across the junction which is called the potential barrier. An external voltage sufficiently large to overcome this potential barrier must be applied in order for a semiconductor diode to conduct.

There are two types of semiconductor materials commonly used in making junction diodes. These are germanium and silicon. Diode action is the same for both types of material; they differ only in their characteristics. Figure 1.1 shows the voltage-current characteristics of a germanium diode and a silicon diode. Two important points on these curves are the forward bias voltage required to initiate conduction and the peak inverse voltage (PIV) which is the reverse voltage that causes the diode to break down and conduct in the reverse direction.



(A) Germanium Diode

(B) Silicon Diode

Figure 1.1 Characteristic Curves

The P-type material of a diode forms the anode and the N-type material forms the cathode. Most diodes use a color band to indicate the cathode terminal. Figure 1.2 shows the schematic symbol of a diode and a forward bias and reverse bias diode circuit.

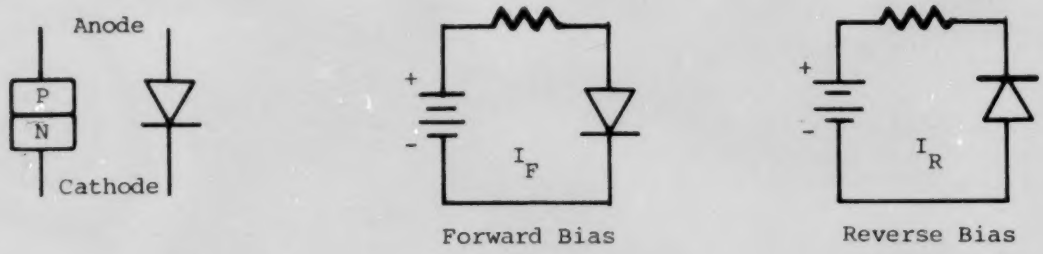


Figure 1.2 Junction Diode and Schematic Symbol

Temperature has an adverse effect on both the forward and reverse current characteristics of a diode. The maximum forward current a diode can safely handle is always given in its specification sheet. Since diodes have some material resistance, heat generated internally due to i^2R power dissipation can destroy the diode unless current is held within specified limits.

Section B - Power Diodes

Diodes which must handle large amounts of current are constructed and packaged so as to minimize the heat generated within the diode and provide a good heat transfer path to dissipate the heat that is generated. These diodes are used primarily in rectifier circuits and output driver circuits for high power DC loads. Power diodes are usually silicon diodes with large junction areas which provide low junction resistance and therefore low power (i^2R) losses under high current conditions. The current carrying capacity of a diode circuit can be doubled by placing two diodes in parallel. The absolute value of peak inverse voltage which two similar diodes connected in series can withstand is twice as great as that of either diode alone.

Power diode specification sheets give power dissipation vs. case temperature curves. These curves provide the information necessary to make the proper choice of diodes for a particular application in a known environment. When operating conditions dictate, it may be necessary to mount power diodes on heat sinks and use either convection or forced air cooling to keep their operating temperature within specified limits. An example of power diodes is shown below.

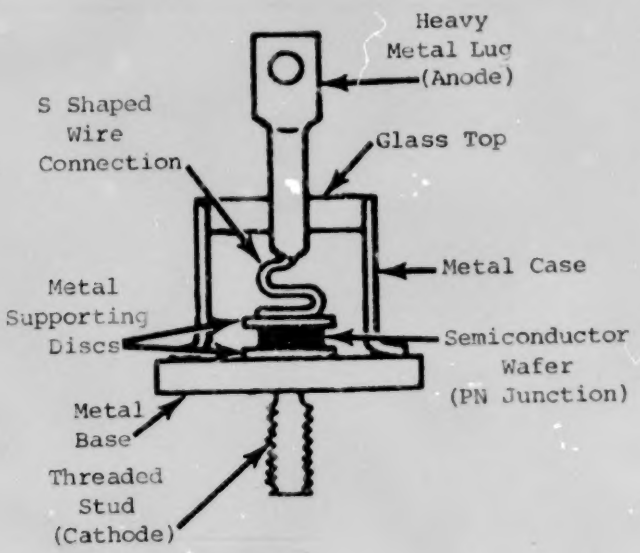


Figure 1.3 Power Diode

Section C - Electrooptical Devices

Electrooptical devices are classified as light sensitive or light emitting devices. Light sensitive devices respond to changes in light intensity by either changing their internal resistance (photoconductive cells) or by generating an output voltage (photovoltaic cells).

Light emitting devices produce light when they are energized by electric current or voltage.

Light Emitting Diodes (LED)

Light emitting diodes are PN junction diodes that emit light due to the release of energy during electron-hole recombination when current is forced through the junction. The color of the emitted light depends on the material of the device. Gallium-arsenide phosphide produces a red light of approximately 660 nm. By adjusting their chemical composition, LED's can be made to emit light of wavelength from 550 to 910 nm.

LED Characteristics

The schematic symbol for an LED is shown in Figure 1.4(c). The relationship between voltage and current on a typical LED is shown in Figure 1.4(a). Figure 1.4(b) shows the relationship between the forward current and the output radiant power. Note that the output radiant power increases linearly with forward current.

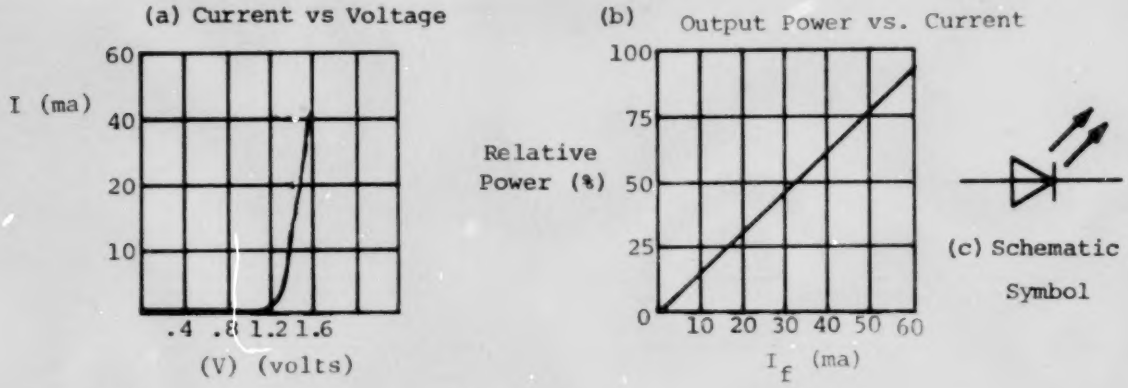


Figure 1.4 LED Characteristics

Applications

In most applications, the LED should be connected in series with a current limiting resistor to prevent its destruction due to excessive current.

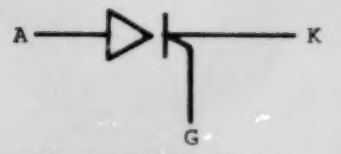
LED's are used extensively as readout indicators, optical couplers, optical limit switches, and punched card and tape readers.

Section D - Thyristors

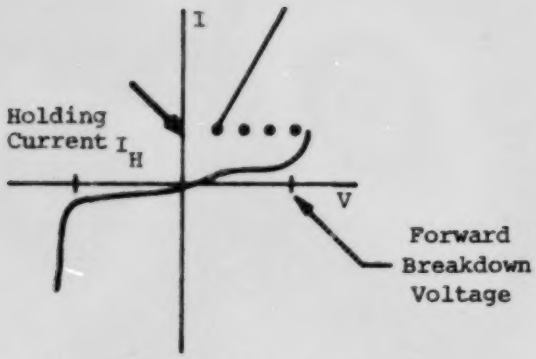
Thyristors are electronically controlled solid state switches. They are used as either an on-off switch or as a momentary interrupt switch to control power being applied to a load. Some thyristors control current flow in one direction only, others control current in both directions. The most widely used thyristors are the silicon controlled rectifier, the bidirectional triode thyristor, the bidirectional trigger diode, the unijunction transistor, and the programmed unijunction transistor. We will discuss only the silicon controlled rectifier (SCR) which is the most widely used thyristor.

Silicon Controlled Rectifier (SCR)

The SCR is a three element solid state device composed of a cathode, an anode and a gate. The forward breakover voltage between the cathode and anode is a function of the applied gate current. Once the forward breakover voltage is reached, the SCR is no longer under control of the gate current but will continue to conduct until the anode current drops below its minimum operating value. The minimum operating current is referred to as the SCR's holding current, I_H. The schematic symbol and operating characteristic curve of a typical SCR is shown in Figure 1.5.



Schematic Symbol of SCR



Operating Characteristics of SCR with Open Gate, $I_G=0$

Figure 1.5

As the gate current of the SCR is increased the forward breakdown voltage decreases. The ability of the gate current to control the breakover point provides the SCR with its variable control characteristics. Figure 1.6 shows the forward characteristic curves of an SCR with several different values of gate current.

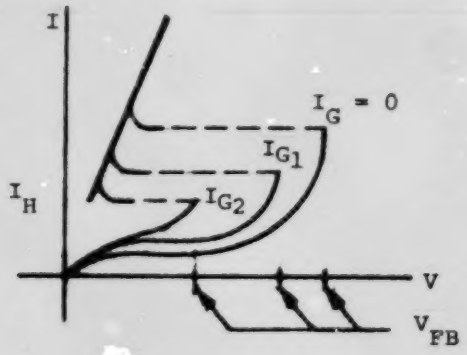


Figure 1.6 SCR Forward Characteristics for Three Values of I_G

Applications

SCR's are used primarily for motor on-off controls and to vary the amount of power applied to a load. Motor speed-torque control and light dimmers are two of the most common applications of SCR control circuits.

Section E - Zener Diodes

Ordinary PN junction diodes will be damaged if operated at voltage levels in excess of their reverse breakdown voltage. A special PN diode designed to operate under these conditions is called a zener diode. Zener diodes are designed to operate with a reverse voltage greater than their breakdown voltage applied across their terminals. In its breakdown region, zener diodes exhibit a very small value of resistance. That is, very large changes in current through the diode cause very small changes in voltage drop across it. Zener diodes are available in a wide range of breakdown voltage levels. The schematic symbol and operating characteristic curve of a zener diode is shown in Figure 1.7.

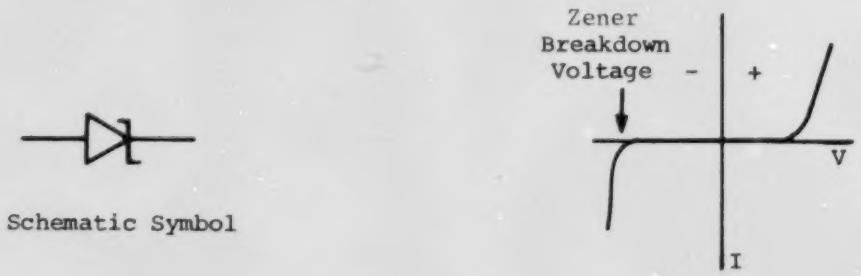


Figure 1.7 - Zener Diode Schematic and Characteristic

Applications

Zener diodes are used extensively in voltage regulating circuits. A resistance should always be placed in series with a zener in order to limit the current through the diode. A typical zener voltage regulator circuit is shown in Figure 1.8.

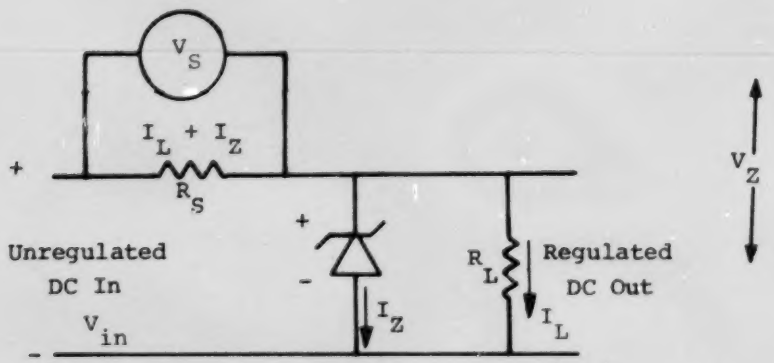


Figure 1.8 - Zener Voltage Regulator

In designing zener regulator circuits, R_s must be selected so that V_s equals V_{in} minus V_z. The zener breakdown voltage and I must be such that the specified maximum current of the zener is not exceeded. The value of R_s can be found from the following equation.

$$R_s = \frac{V_{in} - V_z}{I_L + I_z}$$

The power dissipated in the diode can be determined by the following equation.

$$P_z = V_z \left[\frac{V_{in} - V_z}{R_s} - \frac{V_z}{R_L} \right]$$

P_z must not exceed the specified maximum power rating of the diode.

Section F - Varactor Diodes

When PN junction diodes are reverse biased, the depletion region between the junctions acts as an insulator and separates the P and N sections of the diode as a dielectric separates the plates of a capacitor. A varactor is a diode designed to optimize this capacitance characteristic of a junction diode. As reverse voltage bias across the junction is increased, the depletion layer increases and the capacitance, which is inversely proportional to the distance between the plates, becomes smaller. Figure 1.9 shows a typical capacitance vs voltage curve for a varactor.

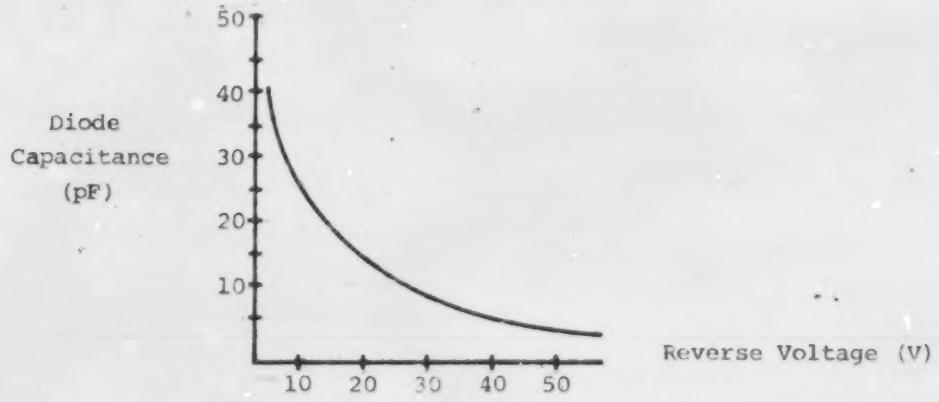


Figure 1.9 Varactor Capacitance vs Voltage Curve

Due to the bulk resistance of the semiconductor material, varactors are effectively an R-C series circuit. As such, they have a measurable Q just as any other capacitor. The Q of the varactor is

$$Q = \frac{X_c}{R} \quad \text{or} \quad Q = \frac{1}{2\pi fCR}$$

Since the capacitance of a varactor changes with voltage, Q must be defined for particular operating conditions if it is to have any useful value. At the frequency that $X_c = R$, Q of the varactor will equal one. The frequency at which this occurs is called the cut-off frequency (f_{co}) of the varactor.

$$f_{co} = \frac{1}{2\pi RC}$$

The schematic symbols for a varactor are shown in Figure 1.10.

Figure 1.10 Schematic Symbol for Varactor

Applications

Varactors can be used in any circuit requiring a variable capacitor. They are used extensively in FM and AM communication circuits where frequency adjusting and control circuits are required. A common application is in a voltage controlled oscillator (VCO) circuit in which the resonant frequency of a tuned circuit is varied by the voltage applied across a varactor in the parallel resonant circuit. A basic circuit for a VCO tuned circuit is shown in Figure 1.11.

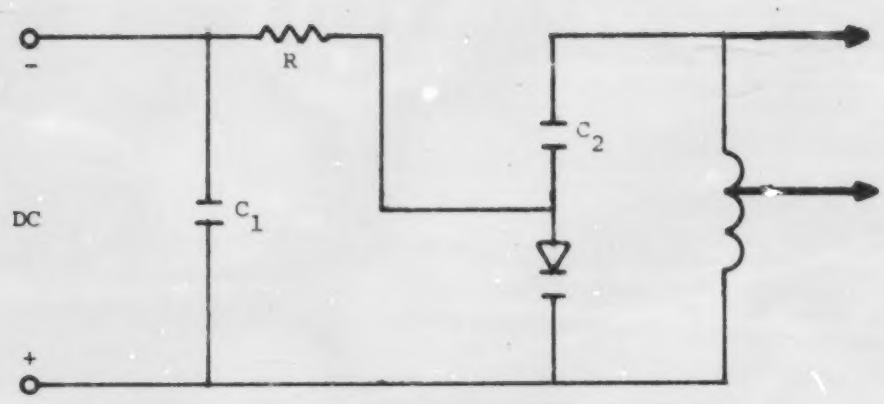


Figure 1.11 Voltage Controlled Tuned Circuit

Capacitor C_1 bypasses AC around the DC source. Capacitor C_2 is much larger than the varactor capacitance and has very little effect on the resonant circuit. It is used to prevent DC from being applied across the inductor.

CHAPTER II

TRANSISTORS

Section A - Introduction

Transistors are essentially two junction diodes connected back to back, that is with either their anodes or cathodes connected together. This forms a three terminal device with the common element, called the base, acting as the control element. The other two terminals are the emitter and collector. If anodes are the common element, the transistor is an NPN transistor. If cathodes are the common element, the transistor is a PNP transistor. Figure 2.1 below shows the diode construction of the two types of bipolar junction transistors (BJT's).

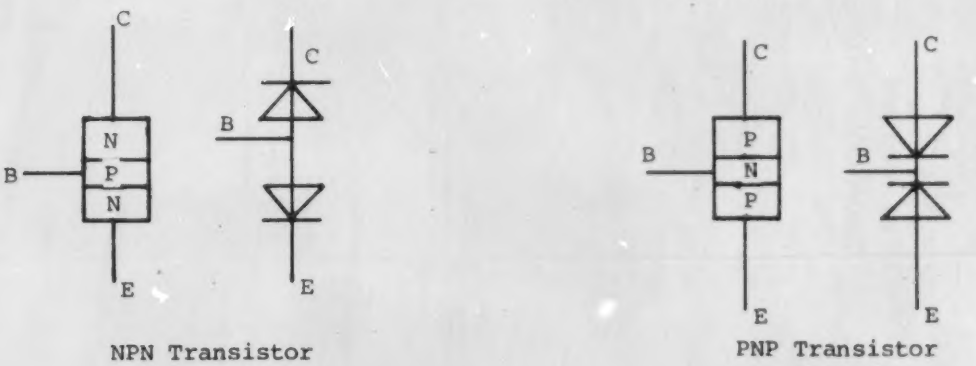


Figure 2.1

The diode construction of bipolar transistors provides a means of checking the transistor for shorts or opens between elements. Each diode should exhibit a low forward resistance and high reverse resistance when checked with an ohmmeter.

Bipolar transistors are constructed so that forward biasing the base to emitter diode permits current to flow between the collector and emitter even though the current flows through the collector diode in the reverse direction. The collector current that flows when the base to emitter diode is forward biased is much greater than, but proportional to, the amount of base current that flows. This proportionality between base current and collector current is the current gain of the transistor and is called BETA (β).

Although transistors are simple to describe, they are relatively difficult to use. They must be biased to operate properly, and the input to output transfer properties of the device must be considered.

Section B - Bipolar Transistors (commonly just called "transistors")

These devices come in two configurations--NPN and PNP. Transistors exhibit between the collector and emitter -- a variable resistance which is controlled by the base to emitter current.

B = Base
E = Emitter
C = Collector

Figure 2.2 - Bipolar Transistors

The arrows were devised for conventional current flow and indicate the direction of positive current flow. An easy way to remember the two symbols is to associate NPN with "not pointing in" and PNP with "pointing in."

Transistor Relationships

Basically, the transistor is a current multiplier and the current at the base (either DC or AC) gets increased by β.

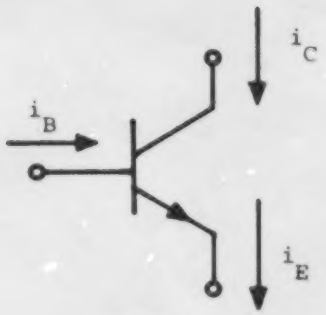
$$i_C = i_B \times \beta \quad \text{or} \quad \beta = \frac{i_C}{i_B}$$

Emitter current is the sum of the base and collector currents.

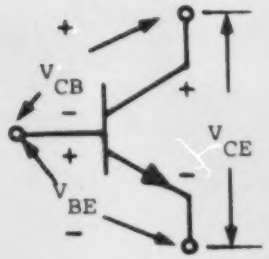
$$i_E = i_B + i_C$$

Applying Kirchoff current and voltage laws to a transistor, it is not difficult to determine the relationships between base, emitter and collector currents, I_B, I_E and I_C, and to determine base emitter and collector voltages V_B, V_E and V_C. There relationships are shown in Figure 2.3.

$$V_{CE} = V_{BE} + V_{CB}$$



$i_E = i_C + i_B$ (a)



$V_{CE} = V_{CB} + V_{BE}$ (b)

Figure 2.3 (a) Base, Collector and Emitter Current
(b) Base, Collector and Emitter Voltage

Biasing

Transistor design and usage requries control of not only the signal processing (AC), but also, the biasing (DC). The DC is necessary because the transistor will not behave properly around its normal at-rest state. It is necessary to force it to some DC state away from zero for proper operation. It is therefore necessary to forward bias the base to emitter causing base current to flow which controls the collector current by way of the transistor characteristic called beta (β).

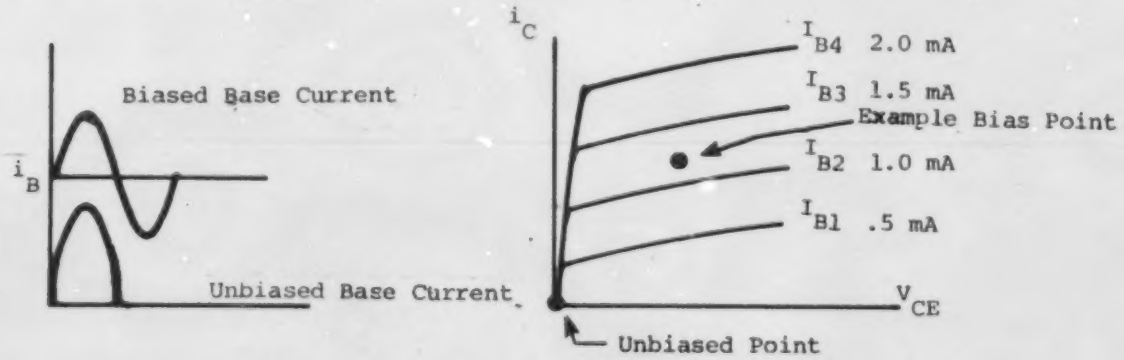


Figure 2.4 - Transistor Biasing

The biasing permits a much greater freedom of electrical movement since the transistor will not function with voltage that reverses polarity or current that reverses direction.

Biasing Concept

The simple (although not very useful) biasing circuit shown in Figure 2.5 makes it easy to see the concept of DC control.

The schematic symbol replaced with the symbol for the NPN structures is shown in Figure 2.6. Base voltage V_{BB} forward biases the base to emitter causing base current to flow; this causes a collector current to flow which is beta times greater than the base current.

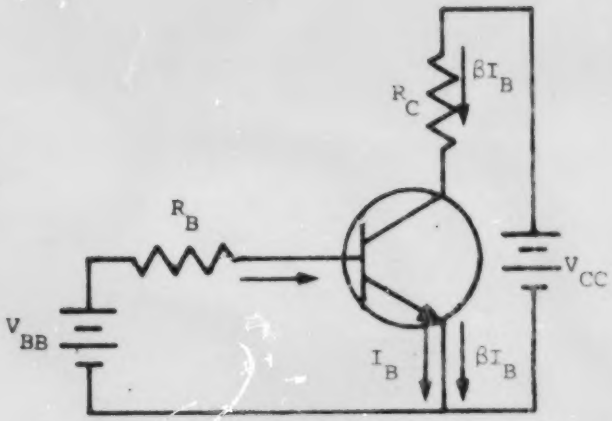


Figure 2.5
Simple Biasing Circuit

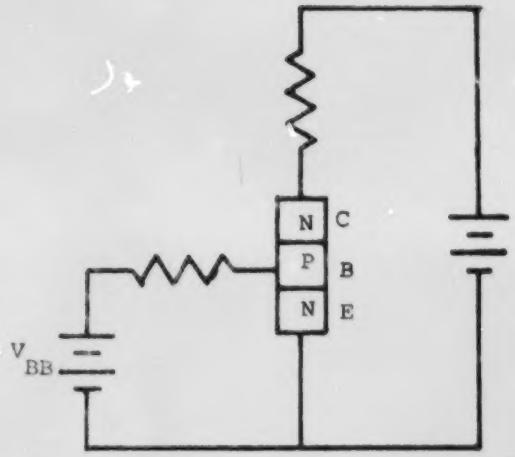


Figure 2.6
Transistor Biasing Circuit Showing Structure

Two conditions must be met to bring the bias point to the operational configuration shown in Figure 2.4. Base current must be large enough to prevent an AC signal from driving it to zero, and the collector to emitter voltage must be such that changes in collector current, due to input signals, will not drive it to its maximum or minimum limit.

Conditions for Transistor Action

In order for a common emitter transistor to provide amplification of a signal applied to its base, the base to the emitter diode must be forward biased and the base to the collector diode must be reverse biased. When forward biased, the base to emitter voltage is approximately 0.7V. The collector voltage is much more positive than the emitter and therefore more positive than the base. This condition reverse biases the base-collector diode.

Normally, transistor circuits do not use a separate voltage source for biasing. Bias voltage is obtained by apply V_{CC} to one of several possible types of resistive networks. A voltage divider circuit shown in Fig. 2.7 is the most practical biasing circuit. Bias voltage and input resistance are determined by replacing the given network with Thevenins equivalent circuit referenced to the base terminal.

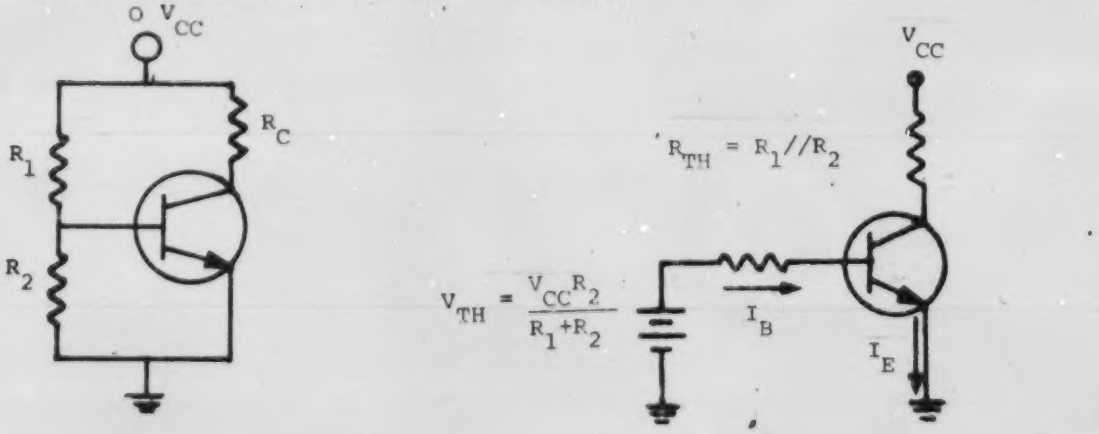
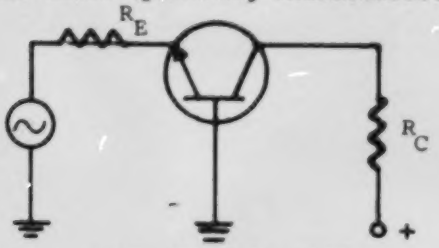


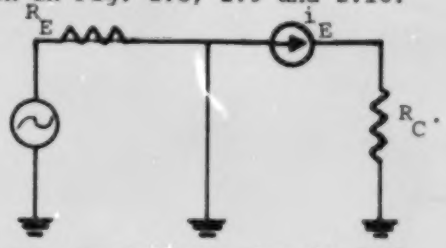
Figure 2.7 - Voltage Divider Bias--Thevenins Equivalent Circuit

Circuit Configurations

Transistors may be connected in three different configurations, each having different input, output, and transfer characteristics. The circuit variations are named for the method of connecting input and output signals to the transistor. Transistors may be connected with a common base, common emitter or common collector. The common element means that the signal input and output are common to that element. The choice of circuit configuration depends on what values of input resistance (R_{in}), output resistance (R_o), current gain (A_i), voltage gain (A_v) and power gain (A_p) are desired. The three types of circuit configurations and their operating characteristics are shown in Fig. 2.8, 2.9 and 2.10.



C.B. Circuit (AC)



C.B. Equivalent Circuit (AC)

$$V_E = i_E R_E$$
$$V_C = i_C R_C$$

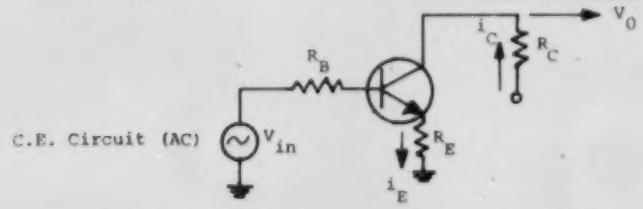
$$A_i = \frac{i_C}{i_E} = \alpha$$

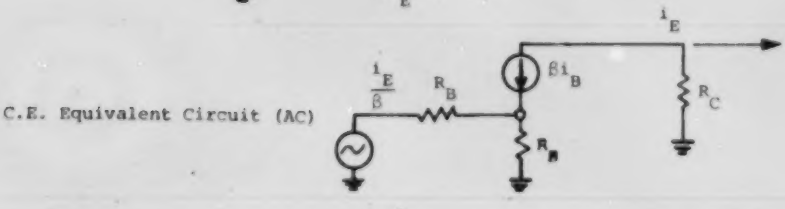
$$Z_{iN} = \frac{V_E}{i_E} = R_E$$

$$A_V = \frac{i_C R_C}{i_E R_E} = \alpha \frac{R_C}{R_E}$$

Figure 2.8 - Common Base Circuit

The common base amplifier can be used as a constant current source or as a current to voltage transducer.





$$V_0 = i_E R_C$$
$$V_{in} = i_E R_E$$
$$Z_{in} = R_B + \beta R_E$$

$$A_i = \frac{i_E}{i_B} \approx \frac{i_C}{i_B} = \beta$$

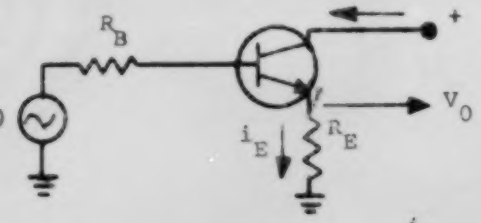
$$A_V = \frac{V_0}{V_{in}} = \frac{R_C}{R_E}$$

$$A_P = A_i \cdot A_V = \beta \frac{R_C}{R_E}$$

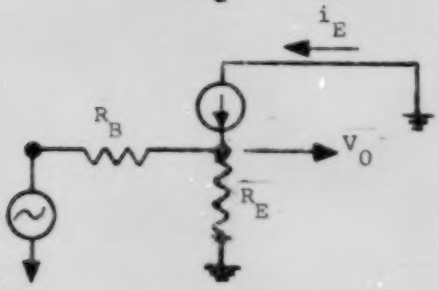
Figure 2.9 - Common Emitter Circuit

Common emitter circuits are the most commonly used amplifier circuits since they provide both current and voltage gain.

C.C. Circuit (AC)



C.C. Equivalent Circuit (AC)



$$V_0 = i_E R_E$$

$$V_{in} = i_E \left(\frac{R_B}{\beta} + R_E \right)$$

$$Z_{in} = R_B + \beta R_E$$

$$A_i = \frac{i_E}{i_B} \approx \beta$$

$$A_V = \frac{V_0}{V_{in}} = \frac{R_E}{R_E + R_B/\beta}$$

$$A_p = A_i \times A_V = \beta$$

Figure 2.10 - Common Collector Circuit

The common collector circuit is called an emitter-follower since the output voltage follows the input voltage with no gain. The circuit is used for impedance matching when it is necessary to couple a high impedance source to a low impedance load.

Section C - Field Effect Transistors (FETs)

A field effect transistor is a high input impedance device. There are two basic types of FETs, the junction FET (JFET) and the MOSFET (for metal-oxide semiconductor). The two types are similar except that the MOSFET has a high resistance layer--the metal oxide--on the input. This oxide layer increases the input impedance and makes possible an additional mode of operation called enhancement mode. The FET, like the bipolar transistor, is a three terminal device. The FET control element is called the gate and the other two elements are the source and drain.

The principal difference between BJTs and FETs is in their control operation. Transistors are current controlled devices and FETs are voltage controlled devices. That is, collector current in a transistor depends on base current, while drain current in a FET depends on gate voltage. BJTs have a low input impedance and the FETs have a high input impedance.

Operating Characteristics

FETs are divided into three operation groups. The JFET operates in the depletion mode only, the normally ON MOSFET operates in both the enhancement and depletion modes, and the normally OFF MOSFET operates in the enhancement only mode.

All FETs are called square law devices which means their transconductance curve is parabolic. When used as a small signal amplifier the FET is acceptably linear because only a small part of the output curve is used. When large signals are amplified, the parabolic relationship between input and output results in nonlinear distortion. This nonlinearity is undesirable in amplifier circuits but is exactly what is needed in special communication circuits called mixers. When two frequencies are mixed in square law devices, output frequencies are produced which are combinations of these frequencies.

Typical characteristic curves of the three types of FETs are shown in Figure 2.11.

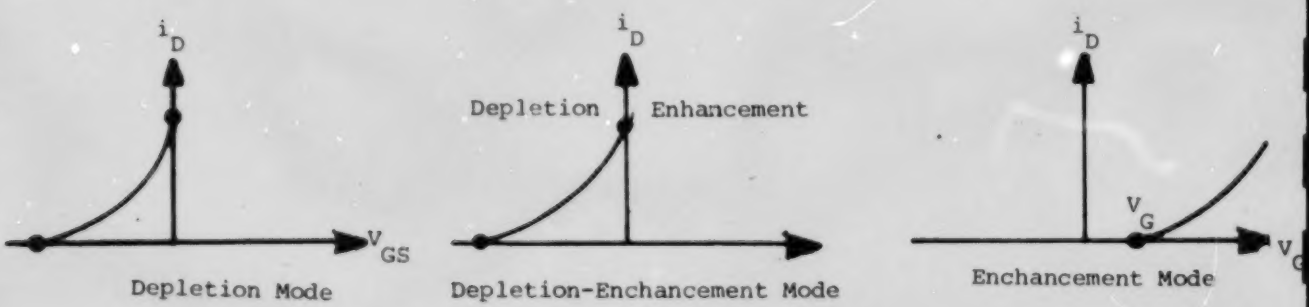


Figure 2.11

Operating Principle

Depletion mode FETs (JFETs) control current flow by depleting the number of carriers in the conducting channel. The number of carriers is reduced by applying a reverse bias voltage to the control gate which must always be reverse biased to prevent base current from flowing.

MOSFETs have insulated gates which prevent gate current from flowing even when the gate is forward biased. Forward biasing the gate produces more carriers in the conduction channel between source and drain. This is referred to as enhancing the carrier channel. When the gate is forward biased, the circuit operates in the enhancement mode. When the gate is reverse biased, the circuit operates in the depletion mode.

Enhancement only (normally off) MOSFETs are constructed so that there is no continuous carrier channel provided. Carriers are made available only by applying a forward bias voltage on the gate, and therefore the circuit can operate only in the enhancement mode. Figure 2.12 shows the schematic symbols of the three types of FETs.

Schematic Symbols for FETs

N Channel FET

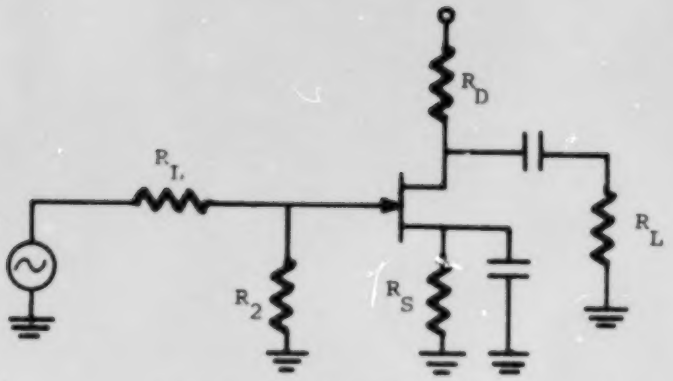
N Channel MOSFET

N Channel Enhancement Only MOSFET

Figure 2.12

Voltage Gain

Transconductance curves shown in Figure 2.11 are a graphical presentation of the relationship between input voltage and output current. The slope of the transconductance curve at any point will give a value of transductance $g_m = \frac{\Delta i_B}{\Delta V_{GS}}$. This relationship of output current to input voltage provides a means of creating a dependent current source which can be used to develop an equivalent AC circuit. A JFET amplifier circuit and its equivalent AC circuit is shown in Figure 2.13.



JFET Amplifier Circuit

Figure 2.13-a

Figure 2.13

If $i_G = 0$, the input voltage $V_{GG} = i_D \left(R_S + \frac{1}{g_m}\right)$ and the output voltage $V_o = i_D R_D$. The voltage gain of the circuit is then

$$A_V = \frac{V_0}{V_{GG}} = \frac{i_D R_D}{i_D \left(R_S + \frac{1}{g_m}\right)} = \frac{R_D}{R_S + \frac{1}{g_m}}$$

If $R_S \geq \frac{1}{g_m}$, then $A_V = \frac{R_D}{R_S}$

If $R_S = 0$, then $A_V = g_m R_D$

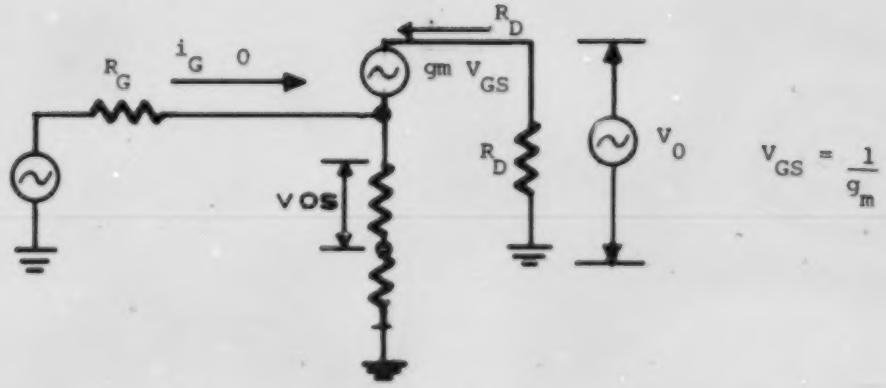


Figure 2.13-b AC Equivalent Circuit

Handling Precautions for MOSFETs

Because the insulating layer that separates the gate and channel of a MOSFET is so very thin, it can be destroyed by too high a voltage between the gate and source. The insulation layer is so fragile that it may even be damaged by static charge that builds up on the leads through improper handling. To minimize the possibility of destroying MOSFETS during shipment and installation, manufacturers usually short the leads of the device together so that static charge cannot build up between leads. Leads should remain shorted together until the device is installed. During installation, the installer should be grounded through a wrist strap and all tools which are applied to the leads should be grounded. MOSFET devices should never be inserted or removed from circuits while power is on.

CHAPTER III

REGULATED POWER SUPPLIES

In the conversion of voltage from AC to DC, there are four regulation considerations:

1. Ripple rejection--the ability to eliminate ripple (the tendency of the output to be affected by the present level of the input waveform). The amount of ripple present is measured by ripple factor (r):

$$\% \, r = \frac{V_{AC} \text{ (rms)} \times 100}{V_{DC} \text{ (ave)}}$$

2. Line regulation--reducing tendency of the output to be affected by the input.

3. Load regulation--reducing the tendency of the load to affect the output. Mathematical definition of load regulation (V.R.):

$$\% \text{ V.R.} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

V_{FL} - voltage under maximum load.

V_{NL} - voltage under no load or minimum load.

4. Temperature regulation--the change of voltage drift that occurs with temperature changes.

Other features of interest include:

1. Foldback current limiting: If too little resistance or even a short circuit is placed on the regulator output, this feature will reduce the amount of current flowing through the device and prevent thermal (i^2R) damage to the regulator.

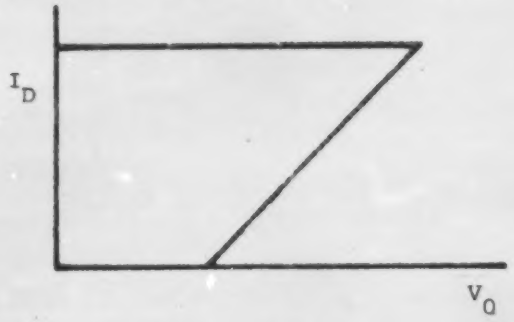


Figure 3.1 Foldback Current Limiter Response

2. Thermal shutdowns: This overload feature coupled with foldback current limiting makes a device virtually faiisafe.

The simplest load regulator uses the zener diode (see figure 3.2).

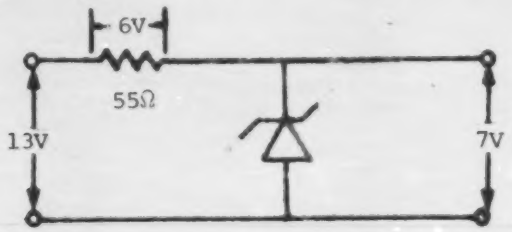


Figure 3.2 Zener Load Regulator

The zener is used to maintain voltage level. As the load requires more current, less current flows through the zener to make up the difference. Knowing the internal resistance of the diode it can be determined how much an increased load will decrease the output voltage. The frequency response of the zener limits this circuit to load current variations in the mid-audio range. If the load current is above the level that removes all of the current from the diode, no regulation occurs.

Design Example

A tape recorder operates at 7 V DC 100 mA. Design a regulator to adapt the recorder to car use. Assume the maximum car voltage to be 13V.

Solution: When there is no load current, the zener needs to be carrying the maximum load current (100 mA) plus some reserve (at least 10 mA). The reserve is necessary because the zener voltage varies more at low current.

$E_r = 13 - 7 = 6V$ Six volts must be dropped across a resistor in series with the zener.

Power dissipated in regulator resistor = EXI = 6 X .11 = .66 watts.

Load power = 7 X .1 = .7 watts.

Find a 1 watt resistor closest to 56Ω. $i^2R = .7$ $R = \frac{700}{12} = 56\Omega$

The zener regulator provides only load regulation. Many of the integrated regulators incorporate all of the features mentioned earlier. The simpler versions, called three-terminal regulators, require no external components and are extremely easy to use (see figure 3.3). These come in two types--positive and negative.

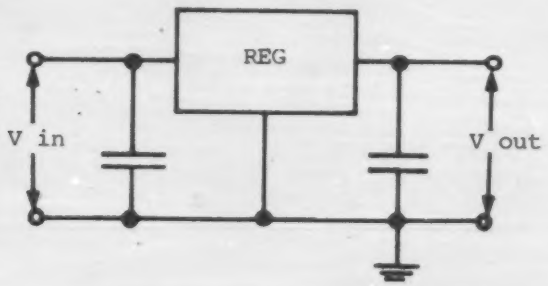
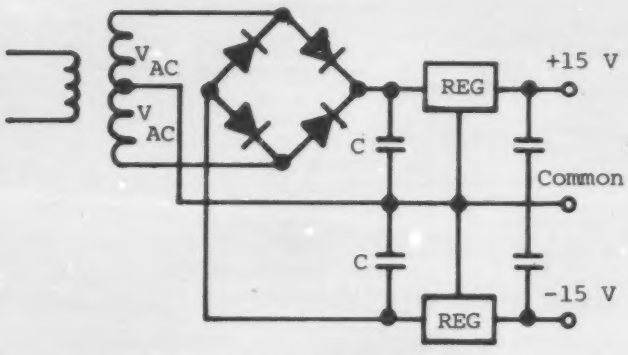


Figure 3.3 - Three-Terminal Regulator

By using a positive and negative power regulator, a bipolar supply can be made (figure 3.4).



$V_{OUT} = \pm 15$ $V_{RECT} = 1.25$

Figure 3.4 - Bipolar Supply

This bipolar function can now be incorporated into one device called dual tracking regulators (eg. UA78T00).

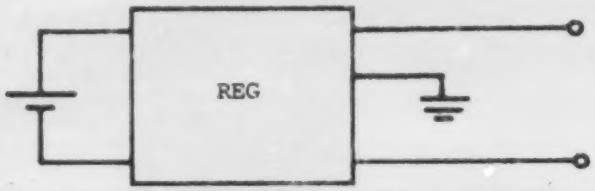


Figure 3.5 - Dual Tracking Regulator

Example: Using the information in Table 3.1 on a 12V positive three-terminal regulator answer the following questions: 1) Even though this device has a specified output level of 12 volts, one might get a device anywhere in what range? (V_{in} = 19V, I out = 0.5A) 2) If in a particular application the average level of the incoming voltage were to vary between 14.5V and 30V, how much would this typically cause the output level to vary? 3) What is the minimum value of the incoming voltage to assure full performance? 4) If the load current were to vary between 250 ma and 750 ma how much variation in output voltage level would typically be experienced? 5) How much is incoming ripple reduced?

Table 3.1

DC ELECTRICAL CHARACTERISTICS I_{OUT} = 500mA, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, T_J = 25°C unless otherwise specified.

PARAMETER	TEST CONDITIONS	7812[1]			7812C[1]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output voltage		V_{IN} = 19V			V_{IN} = 19V			
		11.5	12.0	12.5	11.5	12.0	12.5	V
	Over temp.[1] 5mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	15.5V ≤ V_{IN} ≤ 27V			14.5V ≤ V_{IN} ≤ 27V			
		11.4		12.6	11.4		12.6	V
	Line regulation	14.5V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V			
			10	120		10	240	mV
		16V ≤ V_{IN} ≤ 22V			16V ≤ V_{IN} ≤ 22V			
			3	60		3	120	mV
	Load regulation	5mA ≤ I_{OUT} ≤ 1.5A	12	120		12	240	mV
		250mA ≤ I_{OUT} ≤ 750mA	4	60		4	120	mV
I_{CC}			4.3	6.0		4.3	8.0	mA
ΔI_{CC}	Over temp.[1] with line	15V ≤ V_{IN} ≤ 30V			14.5V ≤ V_{IN} ≤ 30V			
				0.8			1.0	mA
	With load, 5mA ≤ I_{OUT} ≤ 1.0A			0.5			0.5	mA
	Output noise voltage	10Hz ≤ f ≤ 100kHz	75			75		μV
	Voltage drift			48			48	mV/1000hrs.
	Ripple rejection	Over temp.[1] f = 120Hz	15V ≤ V_{IN} ≤ 25V		15V ≤ V_{IN} ≤ 25V			
		61	71		55	71		dB
	Dropout voltage	I_{OUT} = 1.0A	2.0			2.0		V
	Output resistance	f = 1kHz	18			18		mΩ
I_{SC}			350			350		mA
	Peak output current		2.2			2.2		A
V_{OUT}	Output temperature drift	I_{OUT} = 5mA	0°C ≤ T_J ≤ 150°C		0°C ≤ T_J ≤ 125°C			
			-1.0			-1.0		mV/°C

Answers: 1) 11.5V to 12.5V 2) 10mV 3) 14.5V 4) 4mV 5) 71dB

CHAPTER IV

OSCILLATORS

Section A - Introduction

Feedback circuits discussed so far had negative feedback. Oscillators require positive feedback and gain. Negative feedback can result in such improvements as increased linearity, lower output impedance, higher input impedance, increased frequency response, noise reduction and increased stability. Positive feedback coupled with sufficient gain is used to make the circuit unstable, causing it to fall into oscillation. Positive feedback means that some fraction of the output is returned back to the input in such a manner as to increase the overall signal level.

Section B - Wein Bridge Oscillator

Figure 4.1 shows a basic version of a Wein bridge oscillator circuit. The identity of the bridge is obscured in the Figure, but R_3 and R_4 make up the right hand half of the bridge and the other components, the left. The op-amp is connected across the center of the bridge. R_1, R_2, C_1 and C_2 form the frequency adjustment elements and provide the positive feedback path. R_3, R_4, and the op-amp provide the needed gain.

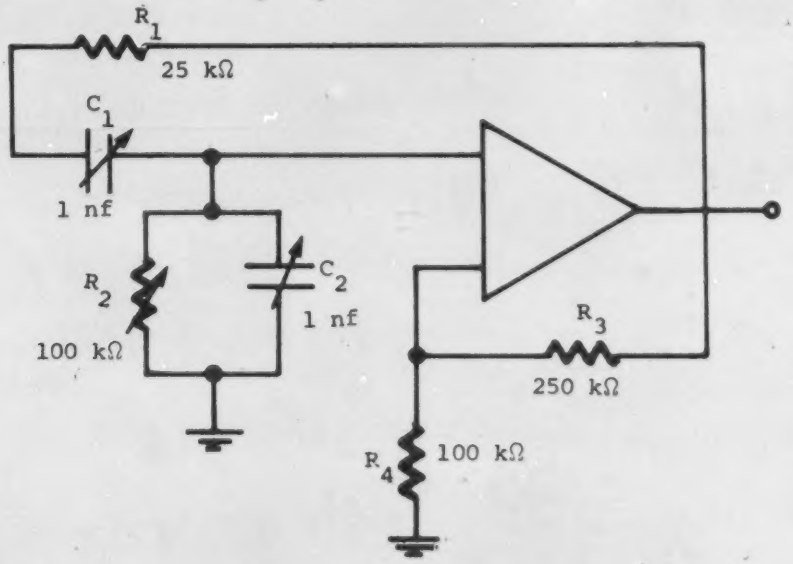


Figure 4.1 - Wein Bridge Oscillator Circuit

The oscillator frequency, f_o, is: $f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

The circuit gain R_3 R_4+1 needs to be at least 2.

Example: For identification of the component, see Figure 4.1.

$$f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} = \frac{1}{6.28\sqrt{(25 \times 10^3)\ (10^{-9})\ (100 \times 10^3)\ (10^{-9})}} = 3.2 \text{ kHz}$$

$$A_v = R_3/R_4 + 1 = \frac{250k\Omega}{100k\Omega} + 1 = 3.5$$

Section C - Crystal Oscillator

A crystal oscillator can have a very stable frequency.

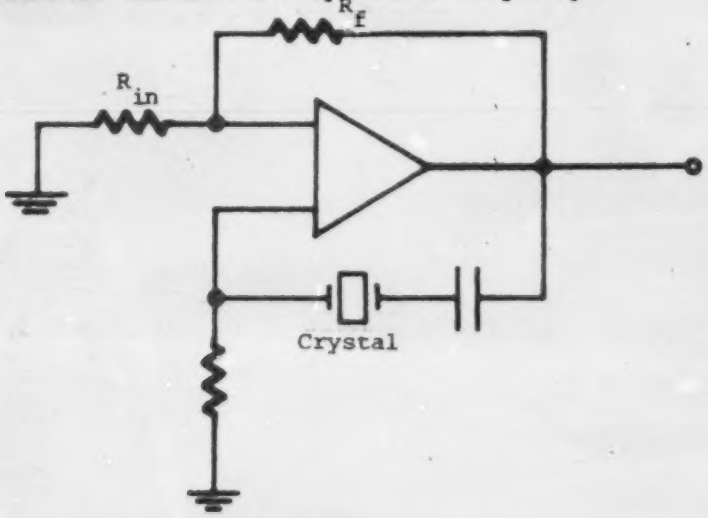


Figure 4.2 - Crystal Oscillator

The crystal behaves as an extremely stable capacitive--inductive circuit providing the positive feedback path. The op-amp with R_{in} and R_f provides the minimum gain needed.

In all of these oscillator circuits a square wave output can be achieved by forcing the circuit to go into saturation on both sides of the output. This can be further squared up by inserting a pair of cathode connected zener diodes from the output to ground. These diodes can be purchased

already connected in a single package. A nice clean sine wave is more difficult to produce. On the one hand, sufficient overall gain must be provided for any output to appear at all. But, if there is too much gain, the output will go into saturation, squaring the output waveform. Some additional circuitry must be provided to ensure keeping the oscillator in this happy medium. A thermistor can be added so that as the amplitude increases the resistance of the thermistor increases, tending to shut down the device. A more sophisticated circuit for this purpose is given in the application section of the CA3140 op-amp spec sheet.

Section D - Multivibrators

There is a wide range of applications for repetitive waveforms which are not sinusoidal. The most widely used class of nonsinusoidal signal generators is the multivibrator. There are three types of multivibrators, all of which operate on the same principle but differ only in the stability of operating states.

The monostable multivibrator, called a one shot, has only one stable state and will remain in that state unless forced into an unstable condition by some externally applied signal. After being forced into an unstable state, a one shot will return to its stable state after a time period established by its internal circuit.

The bistable multivibrator, called a flip-flop, has two stable states and will remain in either stable state unless forced into the other by an externally applied signal.

The astable multivibrator, called a free running multivibrator, has no stable states, but will continually switch from one state to the other. The time required to switch states is controlled by feedback circuits between the two active elements in the unit. The astable multivibrator, being a free running oscillator, is the unit which will be considered in the following section.

Astable Multivibrator

In a sinusoidal oscillator the period of a cycle is determined by the resonant frequency of a tuned circuit. In a non-sinusoidal oscillator the oscillation period is determined by the R-C time constant of feedback circuits between active elements in the oscillator. When the two feedback circuits are identical, the oscillator is a balanced multivibrator, and it will produce a symmetrical square wave output. When the two time constants are different, a nonsymmetrical output is produced. A schematic diagram of an astable multivibrator is shown in Figure 4.3.

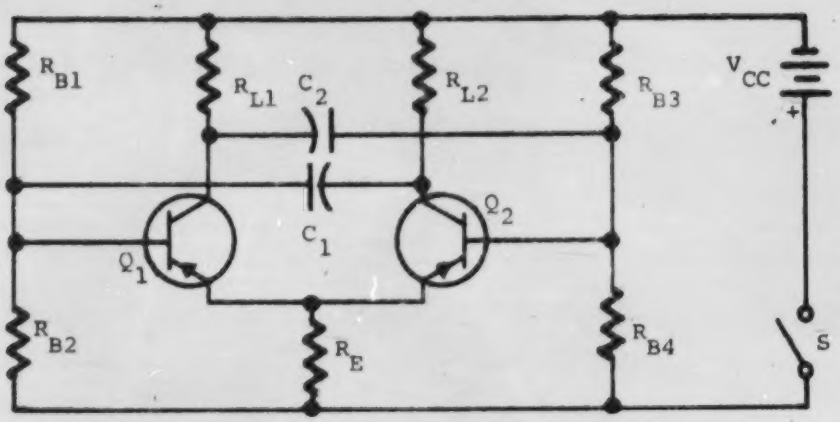


Figure 4.3 Transistor Astable Multivibrator

The time (T_z) that Q_2 remains cut off is a function of $R_{B2}C_1$. When the voltage across C_1 rises above 0.7V, Q_2 turns on and Q_1 is cut off. The time (T_1) that Q_1 remains cut off is a function of $R_{B1}C_2$. When the voltage across C_2 rises above 0.7V, Q_1 turns on and Q_2 is cut off.

Applications

Astable multivibrators are used extensively as square wave or pulse generators for many direct applications. Although its free running frequency is unstable, it can very easily be synchronized to an outside source. The waveform of square wave and pulse signals contains many harmonics which may be used as frequency standards. The multivibrator may also be synchronized to some sub-harmonic of a control frequency and thus act as a frequency divider. The output waveform of a multivibrator may also be modified to produce a sawtooth o tput for CRT sweep control. A practical range of frequencies for a multivibrator is from 1 Hz to approximately 500 kHz.

Section E - Waveform Generators

Integrated circuits which can generate several different types of waveforms, such as square waves, triangular waves, and sine waves, are available at very reasonable prices. The output frequency of these devices is controlled by external circuit components so that oscillators can be made to produce various waveforms over a wide frequency range by simply selecting the appropriate circuit elements.

Most circuits which have a wide range of applications are now available in integrated circuit form. From the standpoint of both economics and simplicity in construction, there is no longer a need for discrete component design of most common circuits.

Figure 4.4 shows a 80338C waveform generator with external circuit elements needed to produce a square wave, triangular wave and sine wave. The frequency of these waveforms is determined by the values of R and C used in the circuit.

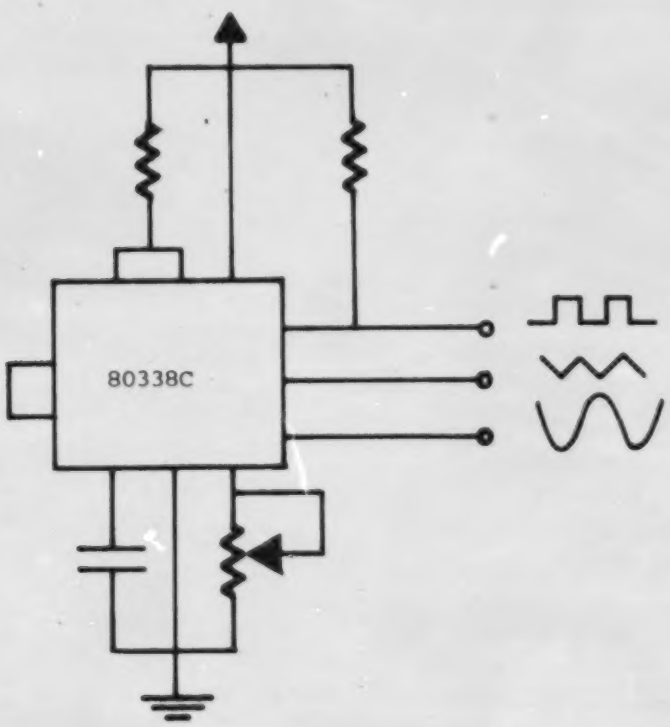


Figure 4.4 Waveform Generator

CHAPTER V

FILTER CIRCUITS

Circuits which attenuate signals of some frequencies more than others are referred to as filters. Three major types of filters, according to their frequency response characteristics, are low pass, high pass, and band pass.

Section A - Low-Pass Filters

A filter which allows lower frequency signals to pass with less attenuation than higher frequencies is called a low-pass filter. A typical low-pass filter is shown in Figure 5.1.

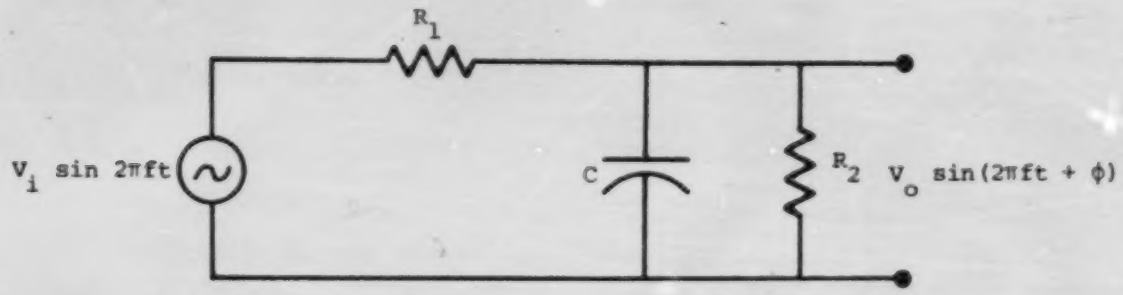


Figure 5.1 Low-pass Filter

The transfer function of a filter is the ratio of the output voltage to input voltage, V_o/V_i. Using the voltage divider rule:

$$Vo = \frac{Vi\ R2}{Z}$$

The frequency response of a filter is usually shown as a plot of log V_o/V_i against log f as in Figure 5.2.

$$Vo = \frac{Vi\ R2}{Z} \qquad \text{then} \qquad \frac{Vo}{Vi} = \frac{R2}{Z}$$

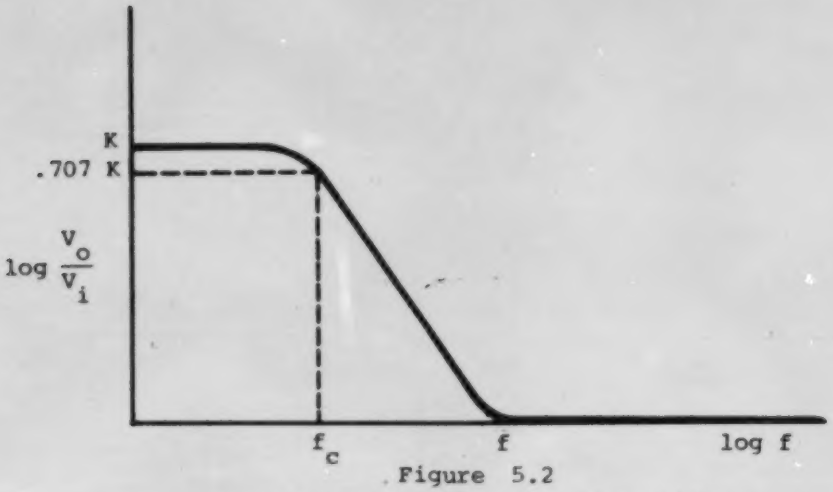


Figure 5.2
Frequency Response of Low-pass Filter

The region of frequencies for which the transfer function has a nearly constant value, K, is called the midband region. The frequency at which the transfer function becomes 0.707 K is called the cut-off frequency, f_c.

The transfer function of the filter circuit in Figure 5.1 is

$$\frac{V_o}{V_i} = \frac{R_2}{\sqrt{(R_1 + R_2)^2 + (R_1 R_2\ 2\pi fC)^2}}$$

The cut-off frequency of the low-pass filter is the frequency for which the reactance equals the resistance and is given by

$$f_c = \frac{R_1 + R_2}{R_1 R_2\ 2\pi C}$$

These filters may be improved by the use of a two-pole filter or by using a two-pole filter with a voltage follower or an inverting amplifier between them as in Figure 5.3.

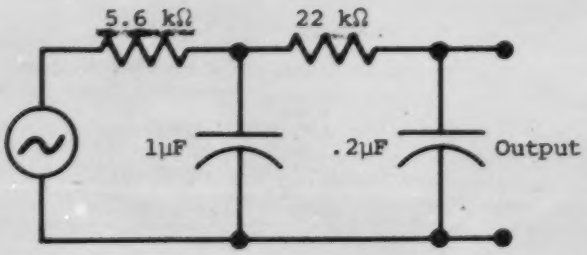


Figure 5.3-a
Two-Pole Low-Pass Filter

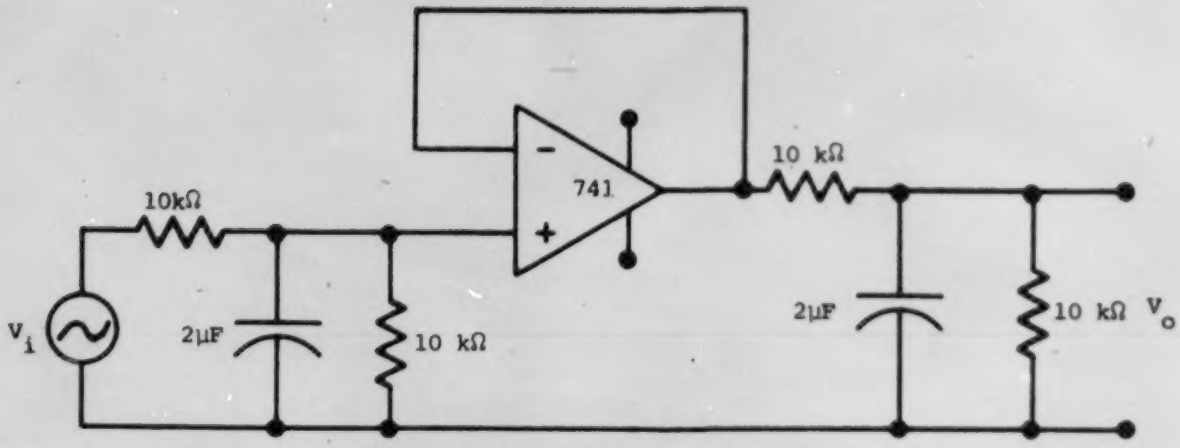


Figure 5.3-b
Two-Section Low-Pass Filter
With Voltage Follower

Example Problems

1. What capacitance is necessary to produce a low-pass filter with a cut-off frequency of 1 kHz for $R_1 = R_2 = 10\ k\Omega$?

   Solution:

$$f_c = \frac{R_1 + R_2}{R_1 R_2\ 2\pi C}$$

$$C = \frac{R_1 + R_2}{R_1 R_2\ 2\pi f}$$

$$= \frac{10^4 + 10^4}{(10^4)\ (10^4)\ 2\pi \times 10^3}$$

$$= 3.183 \times 10^{-8}\ F$$

$$C = 31.8\ pF$$

2. In a low-pass filter $C = 1\mu F$ and $R_2 = 10\ k\Omega$. What value of R_1 is necessary to give a cut-off frequency of 100^2 Hz?

   Solution:

$$f_c = \frac{R_1 + R_2}{R_1 R_2\ 2\pi C}$$

Solving for R_1

$$R_1 = \frac{R_2}{f_c R_2 \, 2\pi C - 1}$$

$$= \frac{10^4}{(10^2)\ (10^4)\ 2\pi\ (10^{-6}) - 1}$$

$$= \frac{10^4}{6.28 - 1}\ \Omega$$

$$R_1 = 1.89 \times 10^3\ \Omega$$

Student Problems

1. What will be the cut-off frequency for a low-pass filter with C = 10 P_F, R_1 = 20 kΩ, and R_2 = 12 kΩ? (2.1 kHz)

2. What capacitance is necessary to produce a low-pass filter with a cut-off frequency of 300 Hz when R_1 = 1.2 kΩ and R_2 = 10 kΩ? (0.5μF)

3. What value of R_1 will produce a cut-off frequency of 60 Hz for a low-pass filter with C = 0.2μF and R_2 = 20 kΩ? (39 kΩ)

LABORATORY

The student should be able to assemble a low-pass filter with any desired cut-off frequency, and then using an oscillator and oscilloscope, determine the frequency response characteristics of the filter.

Section B - High-pass Filter

A filter network such as that in Figure 5.4 will not attenuate high frequency signals as much as those at lower frequencies. This type of filter is a high-pass filter.

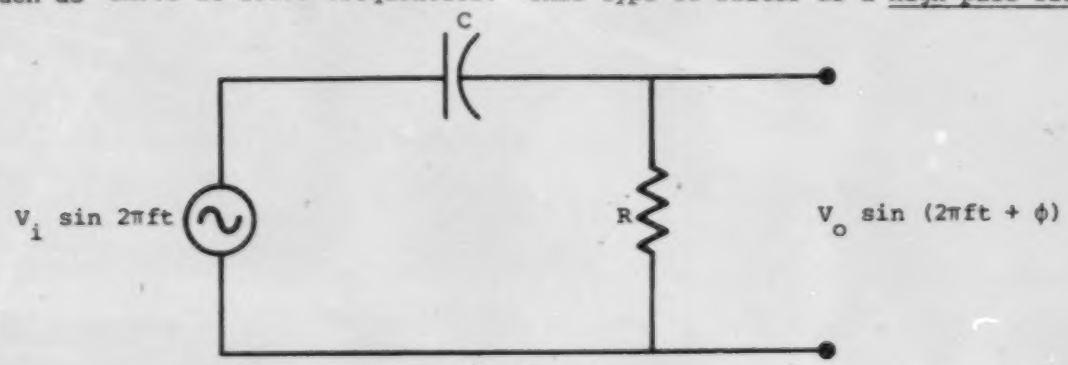


Figure 5.4
High-pass Filter Network

The transfer function for this method is

$$\frac{V_o}{V_i} = \frac{R}{\sqrt{R^2 + \frac{1}{(2\pi fC)^2}}}$$

The frequency response characteristics are shown in Figure 5.5.

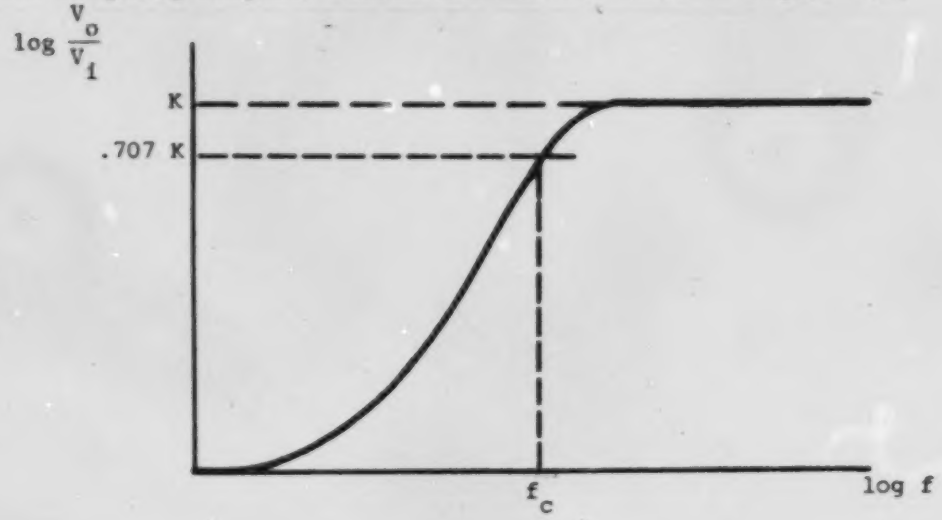


Figure 5.5
Frequency Response Characteristics
for High-Pass Filter

For this high-pass filter, the cut-off frequency is

$$f_c = \frac{1}{2\pi RC}$$

These filter networks may also be coupled together, as in Figure 5.6, to improve filtering or for desired isolation.

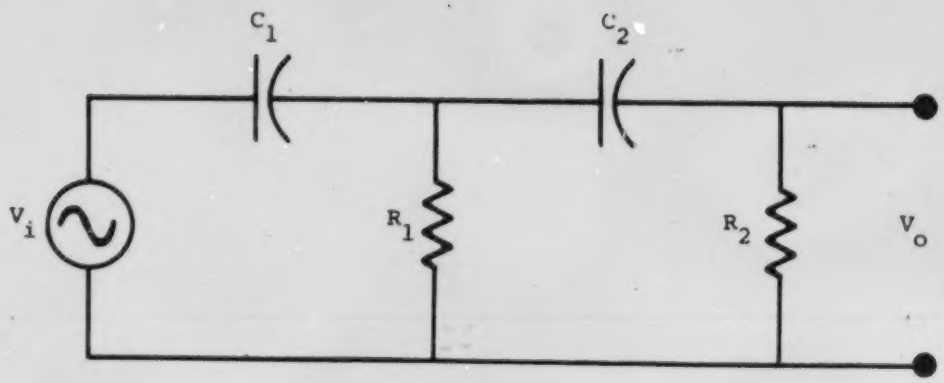


Figure 5.6-a
Two-pole High-pass Filter

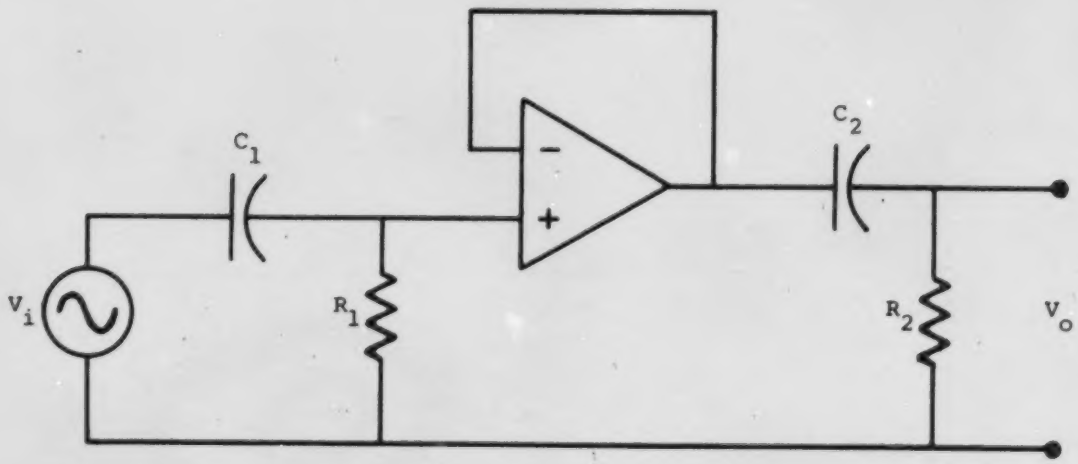


Figure 5.6-b
Two-pole High-pass Filter
with Voltage Follower

Example Problems

1. What capacitance is necessary to produce a high-pass filter with a cut-off frequency of 1 kHz when the resistance is 2.5 kΩ?

   Solution: $f_c = \frac{1}{2\pi RC}$

or $$C = \frac{1}{2\pi R f_c}$$

$$= \frac{1}{2\pi (2.5 \times 10^3)\ \ (10^3)}$$

$$= \frac{1}{1.57 \times 10^7}\ F$$

$$C = 6.37 \times 10^{-8}\ F = 63.7\ pF$$

2. For a 0.5 μF capacitor, what resistance is necessary for a high-pass filter with a cut-off frequency of 100 Hz?

Solution: $$f_c = \frac{1}{2\pi RC}$$

or $$R = \frac{1}{2\pi C f_c}$$

$$= \frac{1}{2\pi (5 \times 10^{-7})\ \ (10^2)}$$

$$R = 3.18 \times 10^3\ \Omega$$

Student Problems

1. What is the cut-off frequency for a high-pass filter with 2 μF capacitance and 5 Ω resistance? (16 kHz)

2. What resistance is necessary to produce a high-pass filter with cut-off frequency 500 Hz if the capacitance is 25 μF? (12.7Ω)

3. A high-pass filter has 1.5 kΩ resistance. What capacitance is necessary to produce a cut-off frequency of 60 Hz? (1.8μF)

LABORATORY

The student should be able to assemble a high-pass filter and determine its frequency response characteristics.

Section C - Band-pass Filter

Low-pass and high-pass filter networks may be combined as in Figure 5.7 to produce a filter which will pass a certain range, or band, of frequency. Such a filter is called a band-pass filter.

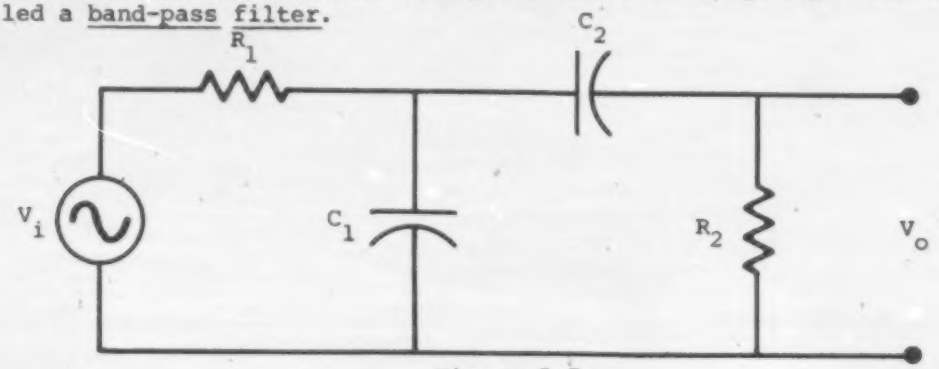


Figure 5.7
Band-pass Filter

This filter can be analyzed by combining the transfer functions of the two filters. The low-pass filter, R_1 and C_1, has a transfer function

$$\frac{V_{o1}}{V_{i1}} = \frac{1}{\sqrt{1 + (2\pi f C_1 R_1)^2}}$$

and establishes the upper cut-off frequency, f_u, at

$$f_u = \frac{1}{2\pi R_1 C_1}$$

R_2 and C_2 make up the high-pass section with transfer function

$$\frac{V_{o2}}{V_{i2}} = \frac{R_2}{\sqrt{R_2^2 + \frac{1}{(2\pi f C_2)^2}}}$$

$$= \frac{1}{\sqrt{1 + \frac{1}{(2\pi f C_2 R_2)^2}}}$$

This circuit establishes the lower cut-off frequency, f_e, at

$$f_e = \frac{1}{2\pi R_2 C_2}$$

Since the output of the low-pass filter is the input of the high-pass filter, $V_{o1} = V_{i2}$, and the transfer function for the entire filter is

$$\frac{V_o}{V_i} = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}} = \frac{1}{\sqrt{1 + \frac{1}{(2\pi f C_2 R_2)^2}}} \frac{1}{\sqrt{1 + (2\pi f C_1 R_1)^2}}$$

The frequency response characteristics for this circuit are shown in Figure 5.8.

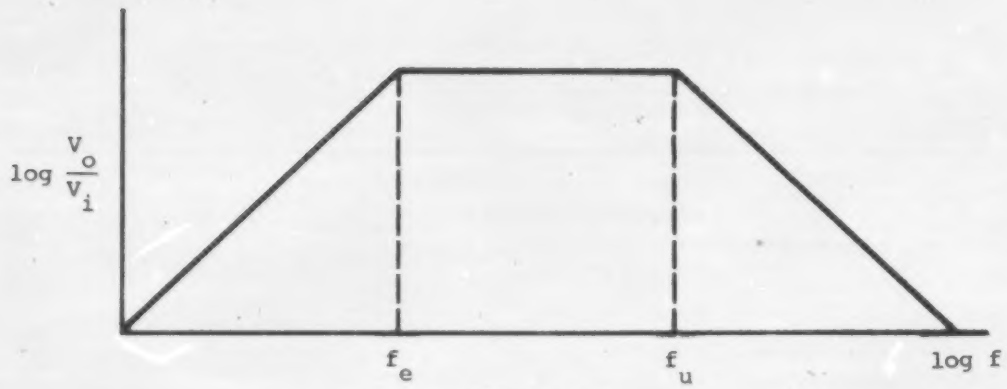


Figure 5.8
Frequency Transfer Characteristics
of Band-Pass Filter

The difference between f_u and f_e is called the bandwidth.

$$\text{bandwidth} = f_u - f_e$$

In many applications it is desirable to have a very small bandwidth - to pass essentially a single frequency. This can be accomplished by setting both f_e and f_u equal to the desired frequency, f_{o1}. In order to achieve this

$$R_1C_1 = R_2C_2 = \frac{1}{2\pi f_o}$$

The resulting frequency response is shown in Figure 5.9.

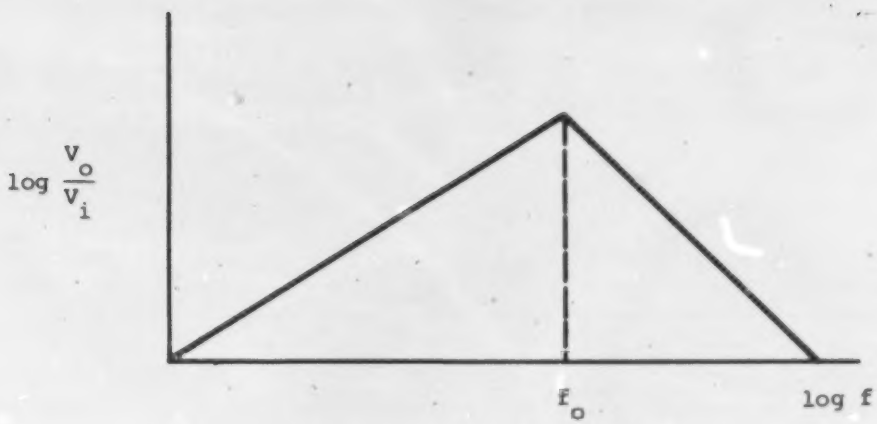


Figure 5.9
Frequency Transfer Characteristics
for Narrow Band-Pass Filter

In order to improve filtering, isolation, and impedance matching these filter sections may be connected by a voltage follower as in Figure 5.10.

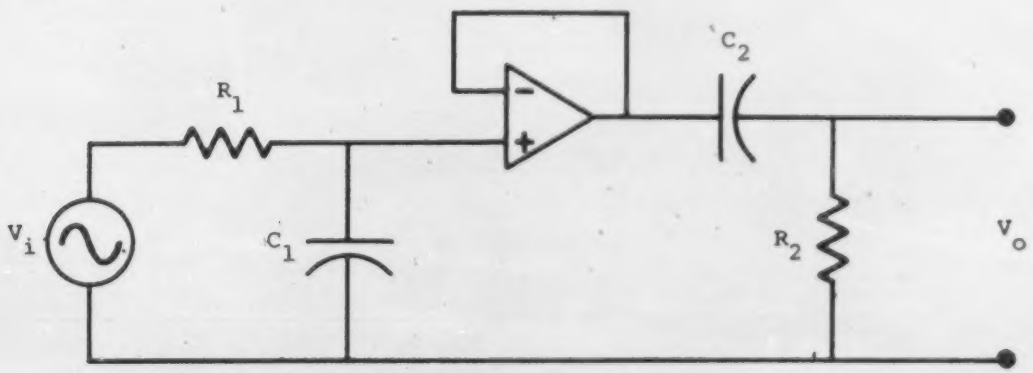


Figure 5.10
Band-pass Filter with Voltage Follower

Solved Problems

1. What values of R_1 and R_2 would be necessary to produce a band-pass filter with cut-off frequencies of 1 kHz and 2 kHz if both C_1 and C_2 are 0.1 μF?

$$f_u = \frac{1}{2\pi R_1 C_1}$$

thus, $R_1 = \frac{1}{2\pi C_1 f_u}$

$$= \frac{1}{2\pi \ (10^{-7} \text{ F})(2 \times 10^{3} \text{ Hz})}$$

$$= \frac{1}{1.26 \times 10^{-3}} \ \Omega$$

$$\boxed{R_1 = 800 \ \Omega}$$

Solve for R_2 $\quad f_e = \frac{1}{2\pi R_2 C_2}$

$$R_2 = \frac{1}{2\pi C_2 f_e}$$

$$= \frac{1}{2\pi \ (10^{-7} \text{ F}) \ \ (10^{3} \text{ Hz})}$$

$$= \frac{1}{6.28 \times 10^{-4}}$$

$$\boxed{R_2 = 1.6 \times 10^{3} \ \Omega}$$

2. What values of R_1 and R_2 will produce a narrow band-pass filter for f_o = 2.5 kHz when both C_1 and C_2 are 0.5 μF?

$$R_1C_1 = R_2C_2 = \frac{1}{2\pi f_o}$$

then, since $C_1 = C_2$;

$$R_1 = R_2 = \frac{1}{2\pi f_o C}$$

$$= \frac{1}{2\pi(2.5 \times 10^{3} \text{ Hz})(5 \times 10^{-7} \text{ F})}$$

$$= \frac{1}{7.85 \times 10^{-3}} \ \Omega$$

$$R_1 = R_2 = 130 \ \Omega$$

Student Problems

1. For a band-pass filter, what values of R_1 and R_2 are necessary for f_u = 1200 Hz and f_e = 1000 Hz if C_1 = 0.2 μF and C_2 = 0.5 μF? (R_1 = 660Ω, R_2 = 320Ω)

2. What values of R_1 and R_2 are necessary to build a narrow band-pass filter for f_o = 20 kHz when C_1 = 0.01 μF and C_2 = 1500 pF? (R_1 = 800Ω, R_2 = 5.3Ω)

Another type of narrow band-pass filter, called a twin-T filter, consists of a network as shown in Figure 5.11. For this filter $f_o = \frac{1}{2\pi RC}$.

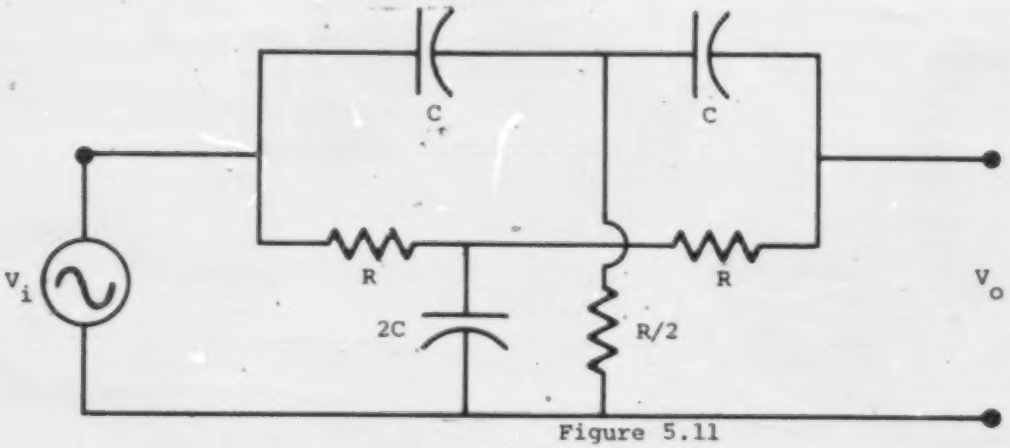


Figure 5.11
Twin-T Filter

This filter has a frequency response characteristic as in Figure 5.12.

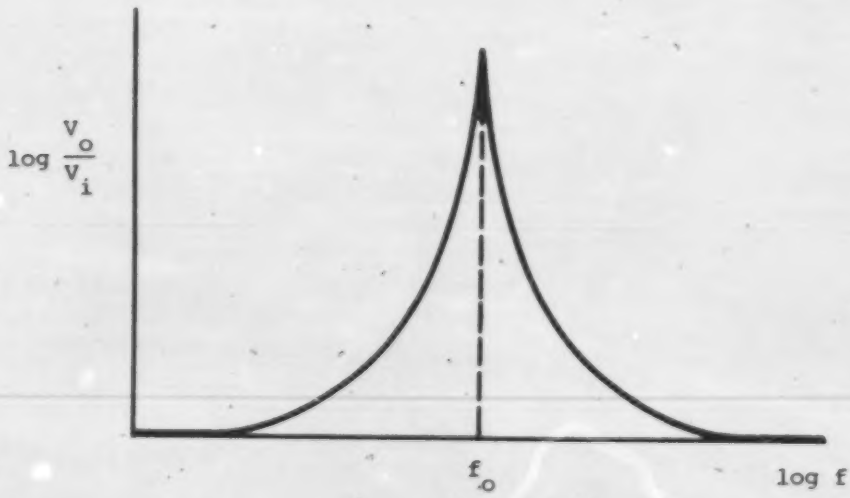


Figure 5.12
Twin-T Filter Transfer Characteristics

The twin-T filter may be used in the feedback loop of an op-amp to produce a band-pass filter as shown in Figure 5.13.

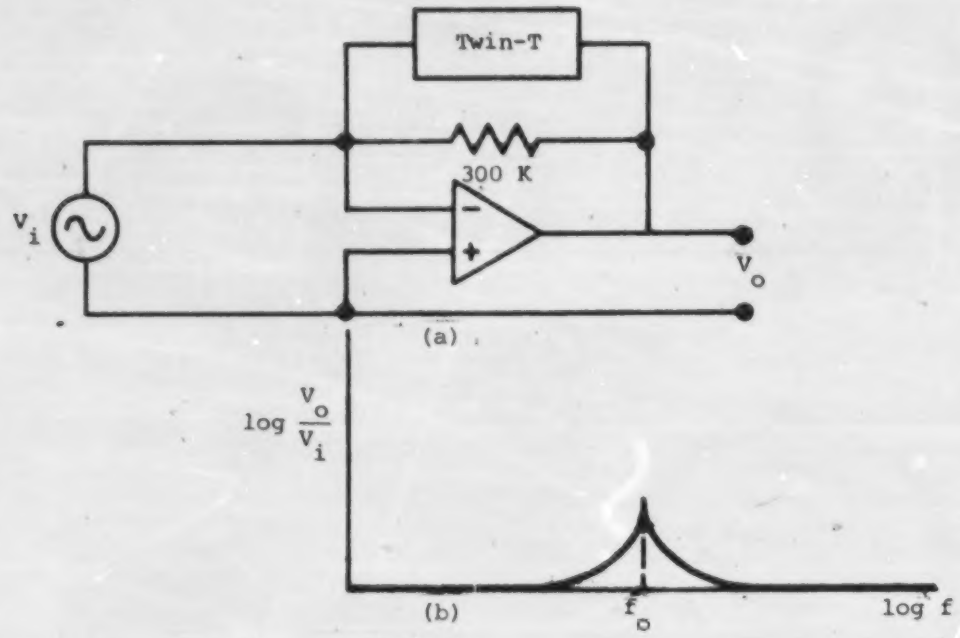


Figure 5.13

a) Op-amp with Twin-T Filter in Feedback

b) Corresponding Transfer Characteristics

A twin-T filter may be used in the input to an op-amp to produce a band reject or notch filter as in Figure 5.14.

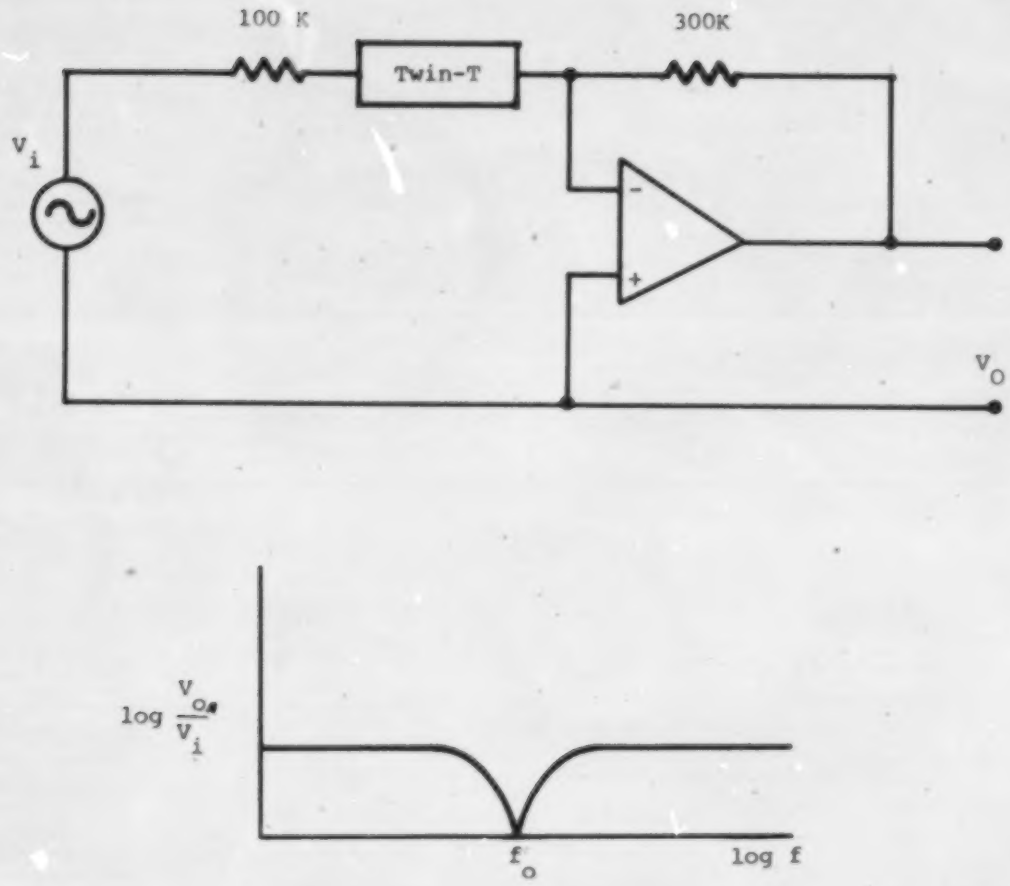


Figure 5.14

Twin-T Filter in Op-amp Circuit to Produce Band-Reject Filter and Corresponding Transfer Characteristics

LABORATORY

The student should be able to build a band-pass filter and determine its frequency response characteristics.

Section D - Integrators and Differentiators

Integrators are used to sum the instantaneous area under a curve. Differentiators are used to develop an output value proportional to the rate of change of an input. Both integrators and differentiators can be built using either passive components, resistors, inductors and capacitors, or operational amplifiers with appropriate feedback circuits.

Integrator Circuits

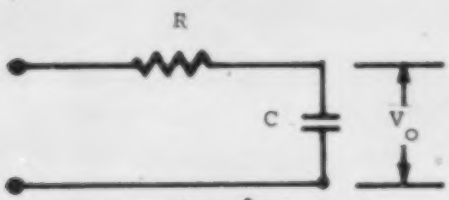


Figure 5.15

Simple RC Integrating Circuit

Equation must be true for all values of t.

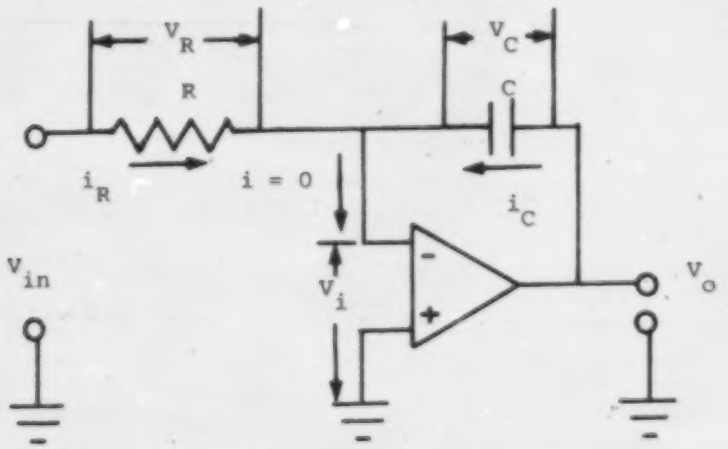
at t = 0 $i_o = \frac{V_{in}}{R}$

$$V_o = -\frac{1}{C}\int i \, dt$$

$$V_o = -\frac{1}{RC}\int V_{in} \, dt$$

$RC > 10T$ Where T is the period of the signal being integrated.

An op amp integrator is show below.



(Figure 5.16)

$$V_o = \frac{-1}{RC}\int_{t_1}^{t_2} V_{in} \, dt$$

The equation for V_o comes from the following circuit relationships.

$$Q = CV \qquad Q = CdV, \qquad i_C = \frac{dQ}{dt} = C\frac{dV_o}{dt}$$

From the op amp characteristics:

$$i_R = -i_C, \quad -i_C = -C\frac{dV_o}{dt} = i_R, \quad V_{in} = V_R$$

Since $V_i = 0, \quad V_o = -V_c, \quad -i_c = -C\frac{dV_o}{dt} = \frac{V_R}{R}$

$$dV_o = -\frac{1}{RC} V_{in}dt$$

Differentiator Circuits

By interchanging the resistor and capacitor of the integrator circuit, a differentiator circuit is formed. Basic differentiator circuits using both passive components and an operational amplifier are shown in figures 5.17 and 5.18.

Figure 5.17,

Simple RC Differentiating Circuit

$$V_o = i_R$$

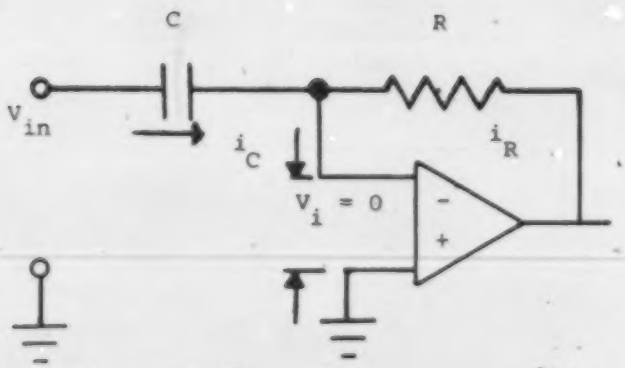
$$\text{at } t = 0, \; i = -C\frac{dV}{dt}$$

$$V_o = -RC\frac{dV_{in}}{dt}$$

$$\frac{V_o}{R} = -C\frac{dV}{dt}$$

In order to perform the function of differentiation, the time constant (RC) of the circuit must be less than 1/10 of the period of the signal being differentiated.

$RC \leq \frac{T}{10}$ Where T is the period of the circuit being differentiated.



$$V_o = -RC\frac{dV_{in}}{dt}$$

$$i_c = C\frac{dV}{dt}$$

Figure 5.18
Differentiator Circuit

From op amp characteristics: $V_{out} = - RC \frac{dV_{in}}{dt}$

Integrators and differentiators are used in analog computer circuits. They may also be used in special applications for filtering and pulse forming circuits.

Problem Example:

1. Sketch the output waveform of an integrator with a square wave input.

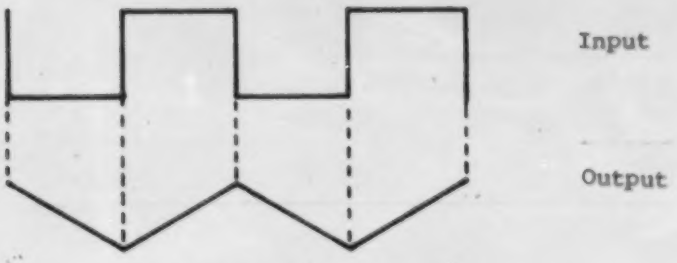


Figure 5.19

2. Sketch the output waveform of a differentiator with a square wave input.

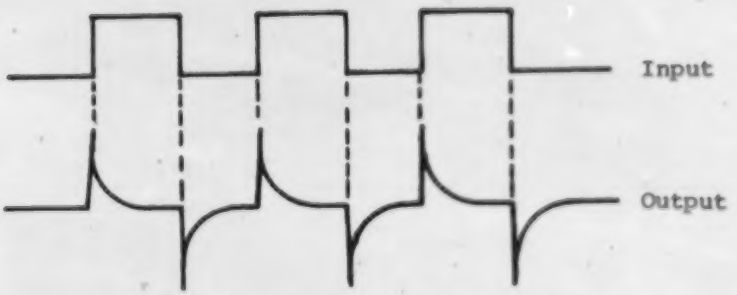
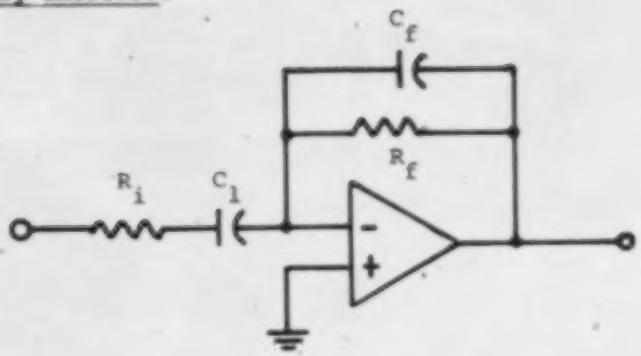


Figure 5.20

Laboratory Exercise:



$$Z_f = \sqrt{R_f^2 + X_{c_f}^2}$$

$$Z_i = \sqrt{R_i^2 + X_{c_i}^2}$$

Figure 5.21
Differentiator/Integrator Using An Op Amp

The relative values of capacitances and resistances in the differentiator and integrator are as shown.

For a differentiator (low frequency): $Z_i = X_{c_i}$, $X_{c_i} > R_i$

$Z_f = R_f$ $R_f > X_{c_f}$

$A_f = -\omega R_f C_i$

For an integrator (high frequency): $Z_i = R_i$

$Z_f = X_{c_f}$

$$A_f = \frac{-1}{\omega R_i C_f}$$

A_f means the voltage gain of the op amp circuit.

Construct the circuit shown in Figure 5.21 to act as: 1) A differentiator for a 1 kHz square wave and, 2) an integrator for a 10 kHz square wave. Sketch the input and output wave for each circuit.

For the differentiator: R_i = 1kΩ C_i = 0.01μf

R_f = 10kΩ C_f = omitted

For the integrator: R_i = 2kΩ C_i = 1μf

R_f = 10k C_f = 0.1μF

CHAPTER VI

DIGITAL CONCEPTS

Section A - Introduction

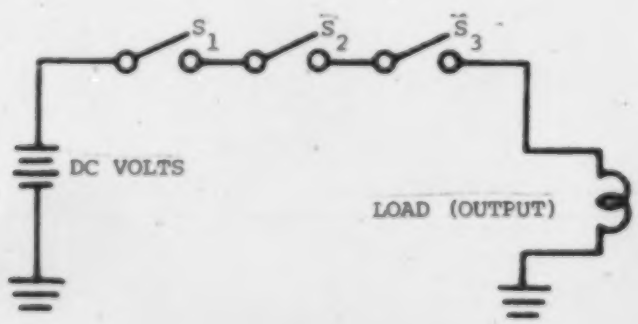
Electronic circuits are divided into two categories--linear and digital. The name linear electronics is given to those electronic systems which have an output proportional to their input over some limited range of values. Digital electronics refers to electronic systems which operate in either of two states, "on" or "off." The on and off states are distinguished by different output voltage levels.

Section B - Switching Circuits

The simplest example of a digital circuit element is a switch. It has only two operational states, on and off. The most basic use of a switch is to permit or prevent the application of power to an electrical system. Switching circuits are called gate because they control signal flow from input to output.

AND Circuit

Logical operations such as AND and OR functions can be performed by using two or more switches. Two or more switches in series form a logical AND circuit. (Figure 6.1)

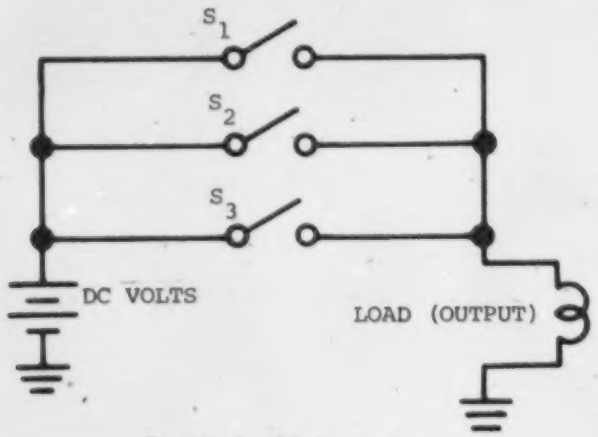


S_1 AND S_2 AND S_3 = L

Figure 6.1 AND Circuit

OR Circuit

Two or more switches in parallel form a logical OR circuit. In the following circuit the load will receive power when either switch S_1, S_2 or S_3 is closed. (Figure 6.2)

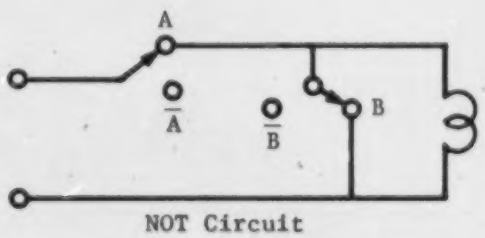


S_1 or S_2 OR S_3 = L

Figure 6.2 OR Circuit

NOT Circuit

Switches can also be used to perform logical negation. That is, the circuit will function only when the switch is NOT closed. A NOT function is indicated by a bar across the top of the switch identification. $\overline{A}$ = NOT A In Figure 6.3 power will be delivered to the load when A is closed and B is NOT closed.

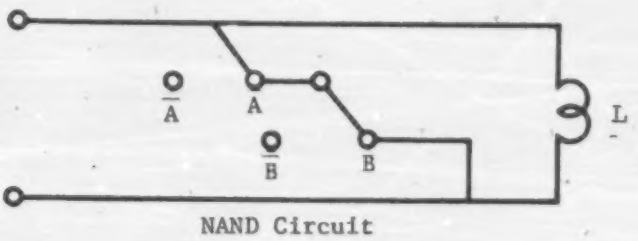


A AND $\overline{B}$ = L

Figure 6.3 NOT Circuit

NAND and NOR Circuits

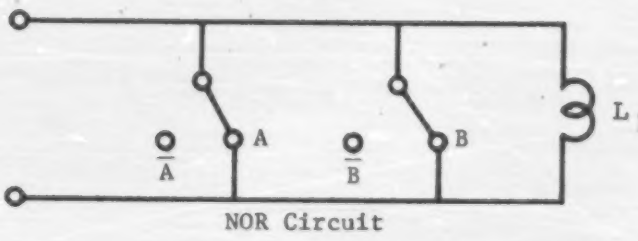
A combination of an AND and a NOT circuit produces a NAND (NOT AND) circuit.
A combination of an OR and a NOT circuit produces a NOR (NOT OR) circuit.



NAND Circuit

NOT (A AND B)

Figure 6.4-a NAND Circuit



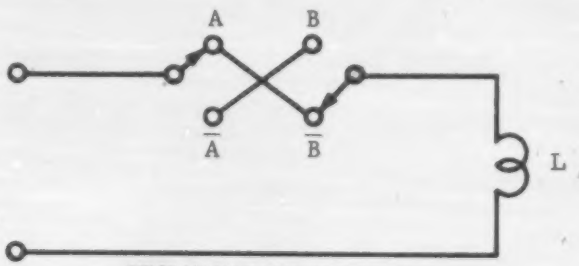
NOR Circuit

NOT (A OR B)

Figure 6.4-b NOR Circuit

EXCLUSIVE OR Circuit

Another logic switching circuit which has many applications is the EXCLUSIVE OR (X OR) circuit. An EXCLUSIVE OR circuit has an output when one and only one switch is on. In the switch circuit shown in Figure 6.5 the load (L) will have power when A only is on or when B only is on. The load will be off when both A and B are off and when both A and B are on.



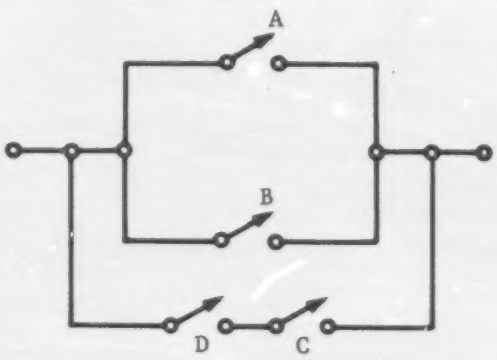
EXCLUSIVE OR Circuit

A AND NOT B OR B AND NOT A

Figure 6.5 EXCLUSIVE OR Circuit

Combination Circuits

Combinations of series and parallel switches form combinational logic circuits. They produce an output only for specific combinations of switch positions. In figure 6.6 power will be delivered to L when A or B or (C and D) are closed.



(A OR B) OR (C AND D)

Figure 6.6 Combination Circuits

Logic Operation Notation

In order to define logical switching operations in an analytical expression, arithmetic operation symbols are used. A logical AND function uses the multiplication symbol (·). A AND B AND C is expressed A·B·C. A logical OR function uses the addition symbol (+). A OR B OR C is expressed A+B+C.

The switch ON state will produce a '1' or "Hi" output. The OFF state will produce a '0' or "Lo" output. "Hi" and "Lo" designation refer to voltage levels for positive logic systems, '1' and '0' designations are binary number notations.

Truth Tables

Single gate operations can be expressed in tabular form for reference and comparisons. Combination tables which show the output from a particular type of gate for each possible input combination are called truth tables. A set of truth tables for an AND and an OR gate are shown below.

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

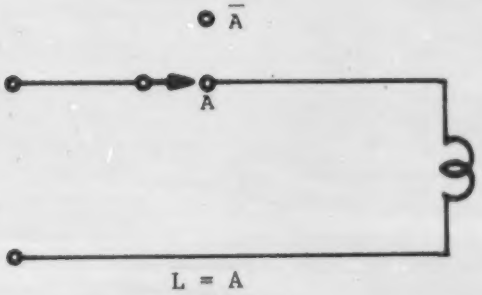
A AND B

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

A OR B

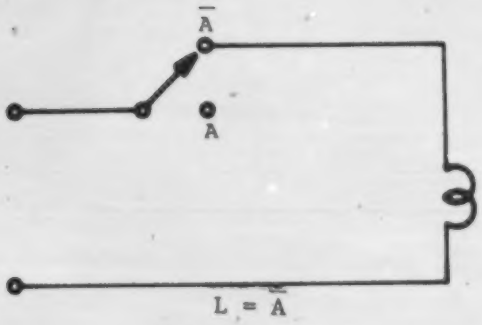
Truth Tables

Several switching circuits and their defining expressions are shown in Figure 6.7.



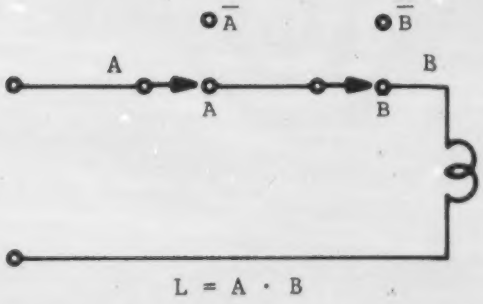
$L = A$

Fig. 6.7-a



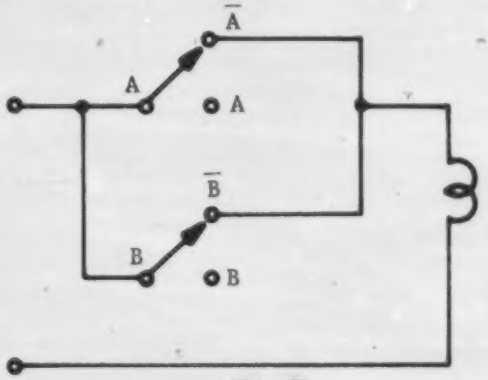
$L = \overline{A}$

Fig. 6.7-b



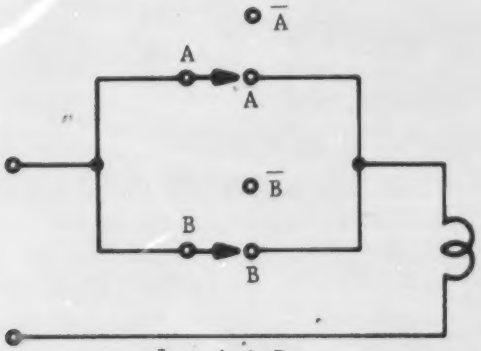
$L = A \cdot B$

Fig. 6.7-c



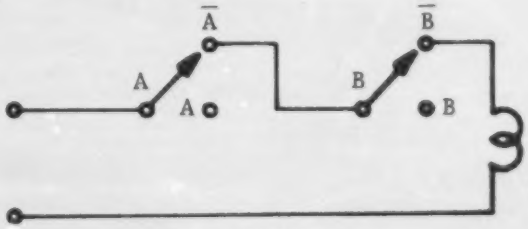
$L = \overline{A} + \overline{B}$

Fig. 6.7-d



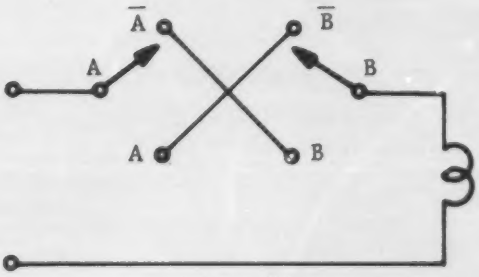
$L = A + B$

Fig. 6.7-e



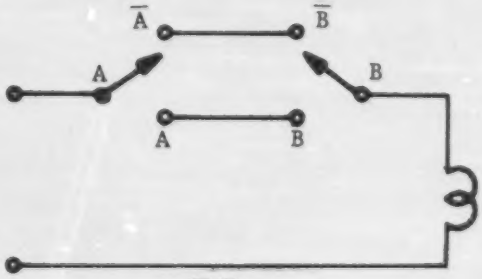
$L = \overline{A} \cdot \overline{B}$

Fig. 6.7-f



$L = \overline{A} \cdot B + \overline{B} \cdot A$

Fig. 6.7-g



$L = \overline{A} \cdot \overline{B} + A \cdot B$

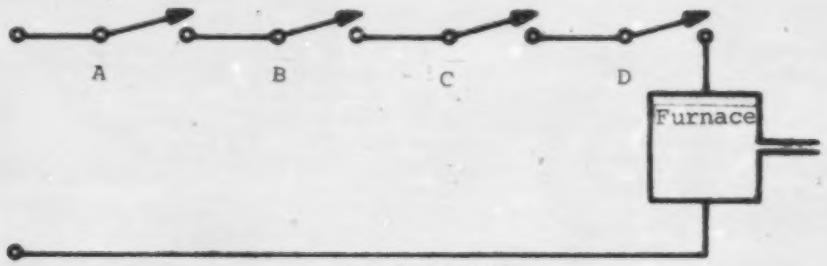
Fig. 6.7-h

Figure 6.7 Switching Circuits

Application of Switching Circuit

Examples:

1. An automatic furnace is an example of a simple switching circuit application. In order for a furnace to turn on, four switches must close: a main power switch, a thermostat control switch, a pilot light safety switch, and a bonnet overtemperature switch. Schematically this circuit is shown below.



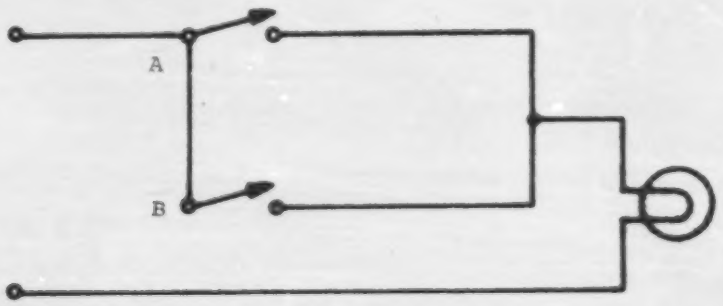
Furnace Control

$F = A \cdot B \cdot C \cdot D$

A = On-Off Switch
B = Thermostat
C = Pilot Safety
D = Bonnet Overtemperature

Figure 6.8 Logical AND Function Application

2. An automobile interior light control is an example of an OR switching circuit. The light will be turned on by either the door switch or an interior light switch.



Light Control

$L = A + B$

A = Door Switch
B = Interior Switch

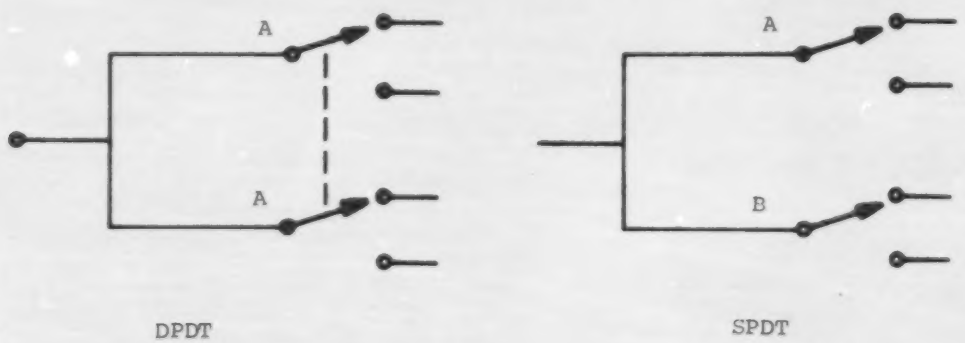
Figure 6.9 Logical OR Function Application

From the simple applications it is easy to imagine the potential of switching circuits in process control. With the use of feedback controls and switching circuits any physical parameter of a system can be regulated. The temperature in a building can be controlled by an automatic furnace as described above when the thermostat switch is controlled by feedback from a temperature sensor. When the temperature rises above the set point, the thermostat switch opens, closing the gas valve. When it drops below the set point, the switch closes, opening the gas valve and restarting the furnace. If the thermostat switch fails in the closed position, uncontrolled heating results until the high temperature cut out switch opens the circuit when the bonnet temperature reaches a preset value.

Combination switching circuits can be defined by logic expressions, depicted with a circuit diagram and implemented by proper installation of hardware. From the logic expressions and circuit diagrams shown previously, it can be seen that in some instances more than one logic expression may be used to define the same function. Figure 6.4-b shows a schematic which depicts the logic expression $\overline{A + B}$ (Not A OR B). It is obvious from the schematic that the expression $\bar{A} \cdot \bar{B}$ (Not A AND Not B) also defines the operation depicted by the schematic. Modification and simplification of logic expressions is the subject of Boolean algebra. The particular relationship shown above, that $\overline{A + B} = \bar{A} \cdot \bar{B}$, is an example of DeMorgan's Theorem in Boolean algebra.

Section C - Combinational Logic

Multiple contact switches operated from a single toggle are shown schematically by joining contact arms with a dashed line or by simply identifying each set of contacts which make contact at the same time by the same switch symbol. This means that if one contact is in the A position all must be in the position and none can be in the $\bar{A}$ position. A double pole double throw (DPDT) switch and a single pole double throw (SPDT) switch may be represented schematically as shown below.



DPDT SPDT

Figure 6.10 Multiple Contact Switches

Multiple contact switches permit the use of one switching operation to effect more than one output. Multiple contact switches must be used in constructing schematics of certain logic expressions.

Logic expressions used to define complex switching operations may have several terms which contain the same switching function. In many instances the original expression may be simplified by identifying redundant operations in the system.

Example of Circuit Simplification

Simplify the expression $(A \cdot B) + A \cdot \overline{B} = L$

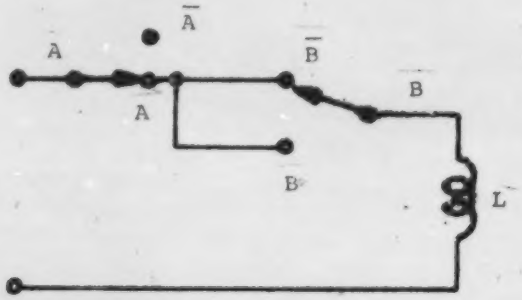


Figure 6.11 Schematic of Expression $(A \cdot B) + A \cdot \overline{B} = L$

If switch A is closed, power will reach the light regardless of which position switch B is in; therefore, the use of switch B is superfluous and can be eliminated. The only switch in the circuit is then A, and the remaining expression becomes A which means power will be delivered to the light through the paths but only when switch A is in position A. The logic expression then reduces to the simple term A = L.

Section D - Truth Tables

A functional table of switching operations can be helpful in determining the output of switching function expressions. When applied to the logic of switching operations, these tables are called Truth Tables. Truth Tables show the output results of all possible input permutations.

A Truth Table of the switching circuits discussed above can be constructed using ON and OFF as the possible input conditions and output results. A Truth Table for an AND and an OR switching circuit is shown below.

Functional Expressions ⟶ A · B = L A + B = L

Switching Function Truth Tables ⟶

A	B	L
OFF	OFF	OFF
ON	OFF	OFF
OFF	ON	OFF
ON	ON	ON

AND

A	B	L
OFF	OFF	OFF
ON	OFF	ON
OFF	ON	ON
ON	ON	ON

OR

When electronic switches are used instead of mechanical switches the voltage level of the input variables determines the switching operation. Input and output conditions are then designated as Hi and Lo instead of On and Off. A voltage level truth table for an AND and an OR gate is shown below.

Functional Expressions ⟶ A · B = L A + B = L

Voltage Level Truth Tables ⟶

A	B	L
Lo	Lo	Lo
Lo	Hi	Lo
Hi	Lo	Lo
Hi	Hi	Hi

AND

A	B	L
Lo	Lo	Lo
Lo	Hi	Hi
Hi	Lo	Hi
Hi	Hi	Hi

OR

All digital devices work on a binary principle, that is, variables in the system can take on only one of two possible states. Using the binary number system to assign numerical values to these states provides another set of notations for Truth Tables. For this notation '0' replaces Off or Lo and '1' replaces On or Hi. A binary truth table for an AND and an OR gate is shown below.

Functional Expressions ⟶ A · B = L A + B = L

Binary Truth Tables ⟶

A	B	L
0	0	0
0	1	0
1	0	0
1	1	1

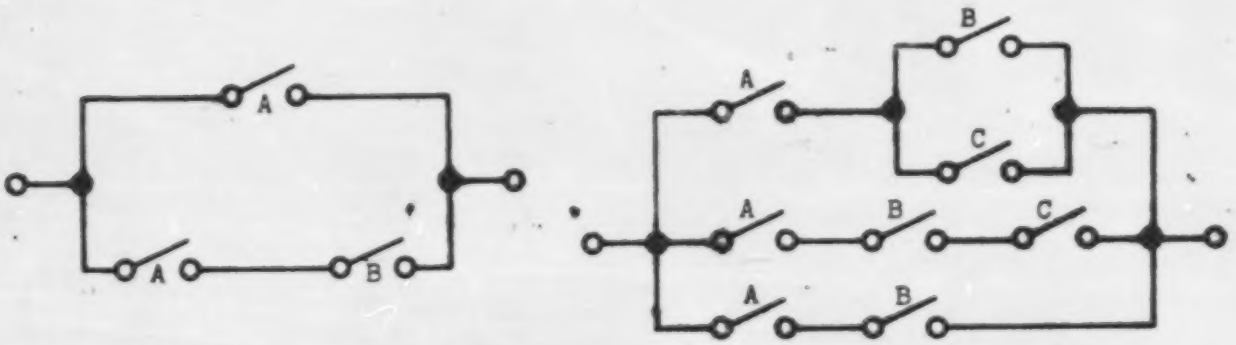
AND

A	B	L
0	0	0
0	1	1
1	0	1
1	1	1

OR

Exercise

Write the expression for the operation of the following two switching circuits.



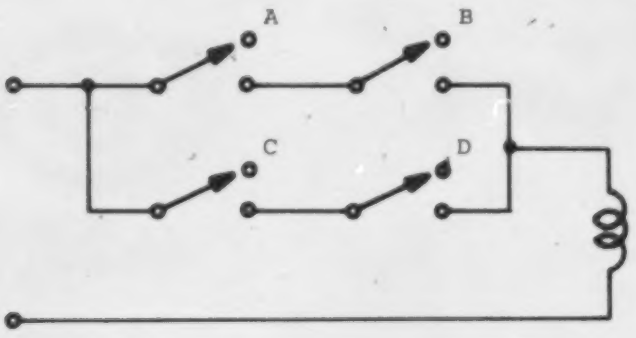
Lab Exercises

Construct switching circuits from logic expressions. Write logic expressions for switching schematics. Simplify switching circuits. Check these results experimentally.

Problems

1. Given a three-way switch which allows a light to be turned on from 2 or more positions, draw a schematic diagram of a switching circuit which will perform this function and write the logic for the circuit.

2. Write the logic expression for the following switching circuit:



3. Sketch a schematic switching diagram for the following logic expression:

$$(A + B) \cdot (C + D) = L$$

4. Write a logic expression other than the one shown to describe the function of Figure 6.7-f.

5. Sketch the schematic for the following expression and from the schematic determine a simplified expression.

$$(A + B) \cdot (\overline{A} + B) \cdot (B + C) = L$$

CHAPTER VII

DIGITAL ELECTRONIC CIRCUITS

The switching circuits shown in Chapter VI control the flow of signals from input to output. These circuits perform a gating function by allowing an output signal to "pass through" the gate only when switches are set in proper positions.

Section A - Logic Gate Symbols

Electronic switching circuits can perform the same function as the manual switches discussed previously.

AND - OR - NOT - XOR Gates

Switching gates are identified with a special symbol for each larger function.

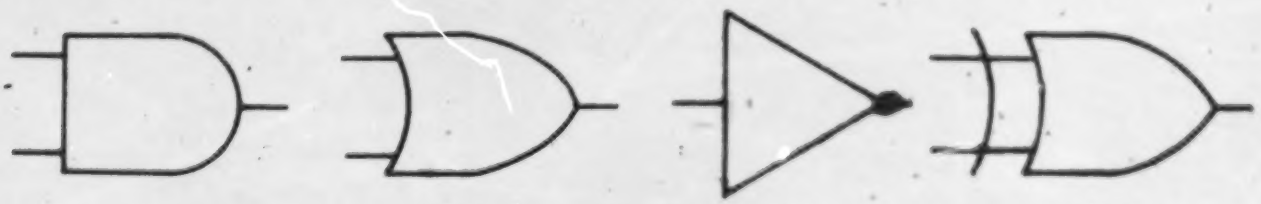
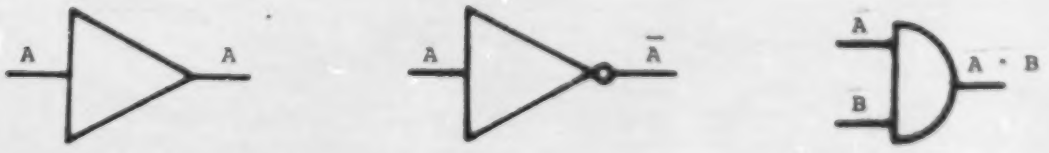


Figure 7.1 AND - OR - NOT - XOR Gates

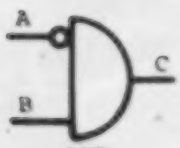
Inverted Input and Output

Gates may be activated by either Hi or Lo input signal levels. Lo activated gates have a small circle at their input terminals. Gate outputs may be either Hi or Lo for a given set of input levels. If a given set of inputs produce a Lo output, a small circle will be attached to the gate output terminal. This small circle symbolizes an inverter. An illustration of the functional meaning of gate notations is given below.



Amplifier Interface | Inverter NOT Function | AND Function

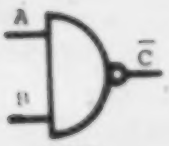
Figure 7.2



AND

$\overline{A} \cdot B = C$

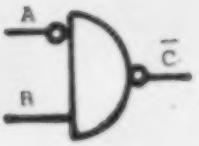
A(LO) AND B(HI) = C
AND gate



NAND

$A \cdot B = \overline{C}$

A (HI) AND B(HI) = C (LO)
inverted AND (NAND) gate



NOR

$\overline{A} + B = \overline{C}$

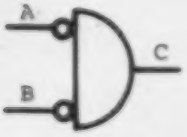
A(LO) OR B(HI) = C(LO)
inverted OR (NOR) gate

Figure 7.3

AND gates and OR gates with an inverted output are called NAND and NOR gates, respectively. NAND stands for NOT AND and NOR stands for NOT OR.

Example Problem

From a truth table determine the input - output functional relationships of the gates shown.



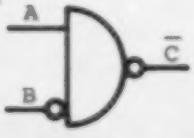
AND

(A)

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

A(LO) · B(LO) = C(HI)

$\overline{A} \cdot \overline{B} = C$
$0 \cdot 0 = 1$



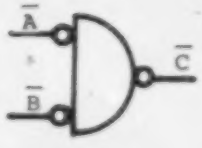
NAND

(B)

A	B	C
0	0	1
0	1	1
1	0	0
1	1	1

A(HI) · B(LO) = C(LO)

$A \cdot \overline{B} = \overline{C}$
$1 \cdot 0 = 0$

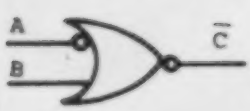


NAND

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

A(LO) · B(LO) = C(LO)

$\overline{A} \cdot \overline{B} = \overline{C}$
$0 \cdot 0 = 0$



A	B	C
0	0	1
0	1	0
1	0	1
1	1	1

A(LO)OR B(HI) = C(LO)

$\overline{A} + B = \overline{C}$
$0 + 1 = 0$

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

A(LO) OR B(LO) = C(HI)

$\overline{A} + \overline{B} = C$
$0 + 0 = 1$

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

A(HI) OR B (HI) = C(LO)

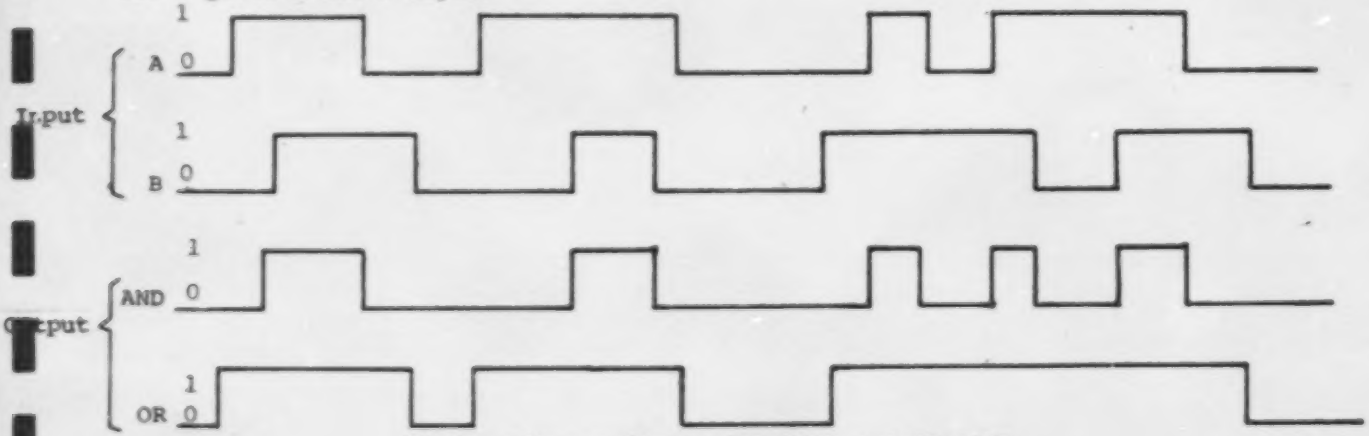
$A + B = \overline{C}$
$1 + 1 = 0$

Section B - Timing Diagrams

Since switching circuit input signals come from a variety of sources, such as clocks and counters which are constantly changing states, an understanding of when switching operations take place is essential to the understanding of the overall operation of digital circuits. Timing diagrams provide a means of determining the output of a particular gate at any given time if the signal input timing chain is given.

Example

The following timing diagram shows the output of an AND gate and an OR gate for a given A and B input.



Timing Diagram for an AND GATE and OR GATE

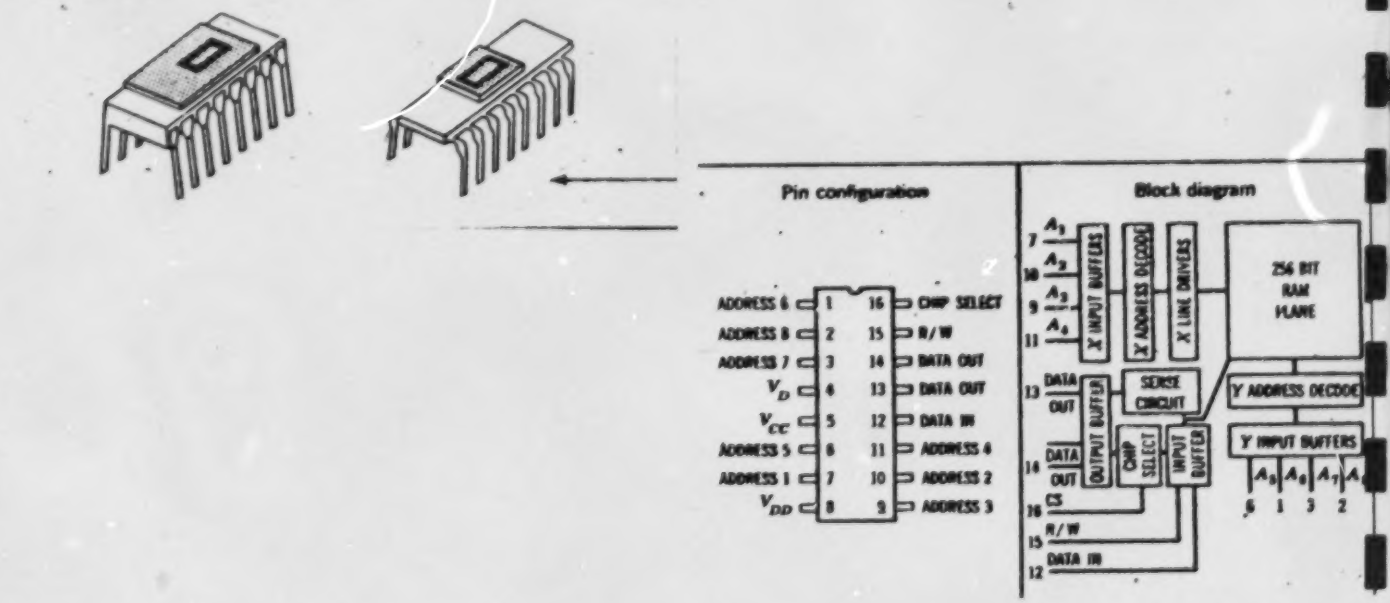
The "AND" gate output is in the "1" state only when A and B are 1.
The "OR" gate output is in the "1" state when A or B is 1.

Section C - Integrated Circuits

Vacuum tubes were used in the past to perform switching and amplifying functions. Tubes have been replaced with solid state devices which provide advantages in size and power requirements. Modern technology is constantly improving on the physical size, power requirements, switching time and noise immunity of solid state circuits.

Special fabrication techniques make it possible to build complete systems on a single base called a chip. Devices which have many active and passive circuit components on a single chip are called Integrated Circuits. Integrated circuits fall into three categories distinguished by the number of circuits constructed on a single chip. Small scale integration (SSI) chips contain from 1 to 11 gates. Medium scale integration chips (MSI) contain 12 to 99 gates and large scale integration (LSI) chips contain over 100 gates.

The availability, reliability and low cost of digital IC's has made it possible to construct sophisticated logic circuits with a minimum of hardware and design effort. It is no longer necessary to construct logic circuits from discrete components, since each IC logic family has all of the major operational circuits built into IC chips. A logic system of any type desired can be assembled by properly combining available IC packages.



LARGE SCALE INTEGRATION - INTEGRATED CIRCUIT

Figure 7.4

Different approaches to the problems of improving design parameters of IC's have led to the development of several different types of logic circuits all of which perform the same basic functions. They differ only in voltage levels, switching times and power requirements. Circuits from these various logic families may be intermixed in a single system if precautions are taken to assure compatibility between systems. This is accomplished by using interface circuits which modify operating parameters. A list of various logic families is given on the following page along with a table of their performance characteristics.

LOGIC FAMILY	POWER/GATE (watts)	PROPAGATION DELAYS- (ns)	FAN OUT	NOISE IMMUNITY	SUPPLY VOLTAGE	BASIC GATE LOGIC
RTL Resistor Transistor Logic	$12X10^{-3}$	50	5	8V	+3.6V	NOR
DTL Diode Transistor Logic	$12X10^{-3}$	30	8	.4V	+5	NAND
TTL Transistor Transistor Logic	$12X10^{-3}$	12	10	.4V	+5	NAND
CMOS Complementary Metal Oxide Semiconductor	$50X10^{-6}$	50	50+	1/3 of VCC	+3,+18V	NOR/NAND
ECL Electron Coupled Logic	$50X10^{-3}$	4	25	Variable	-5.2V	OR/NOR

TTL Dip Circuits

In our discussion of hardware and circuit applications we will use IC's with dual inline pins of the TTL family.

TTL is an abbreviation for Transistor-Transistor-Logic which is a descriptive title of the internal circuitry used in the chip. TTL packages are very inexpensive and cover the whole gamit of logic operations.

For example, below is the schematic diagram of a standard TTL, QUAD NAND Gate (7400).

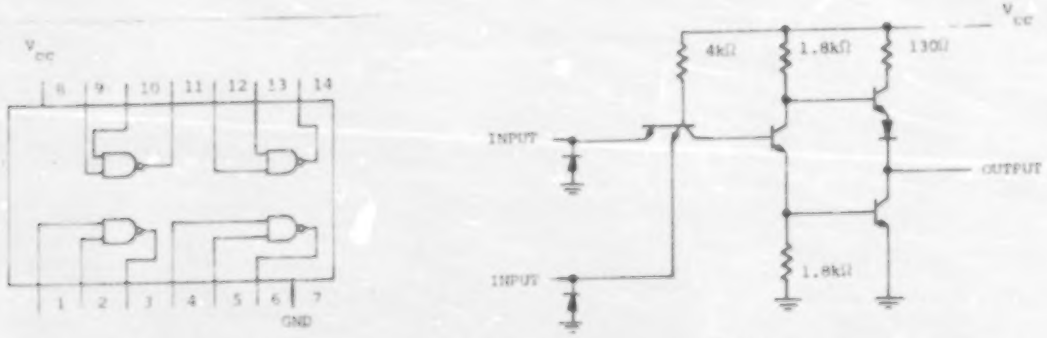


Figure 7.5 - TTL 7400

In this chip (about 1/4 the size shown) are 4 independent NAND gates that may be used singly or in combinations.

All TTL logic requires a supply voltage of +5V. Nominally, a logical "1" for this family is +5V and a "0" is 0V. However, the circuits actually operate with 0's as high as .2 V and 1's as low as 2 volts.

Laboratory

Using 7400 series AND, OR, NAND, and NOR gates, develop truth tables for the various logic circuits. If the output voltage level is above 2V, place a 1 in the data table. If the output is below .2V, place a 0 in the table.

Problems

1. Using the following TTL IC's, verify their truth tables. Make a table of output vs input voltages for each of the following gates and compare the resultant outputs to the truth table.

   7402 QUAD 2 input NOR gate

   7432 QUAD 2 input OR gate

   7408 QUAD 2 input AND gate

   7404 HEX inverter

Multivibrator

Logic gate circuits respond only to the immediate condition of their inputs. When any one input changes, the output responds to that change. There are other logic circuits with outputs controlled by their input but which maintain the same output even when the input is removed. Their output changes when activated by a switching pulse called a trigger pulse. These devices are called multivibrators. There are three classifications of multivibrators--astable, bistable, and monostable.

Astable Multivibrator--Astable or free running multivibrators switch alternately between Lo to Hi states. Switching rates are determined by the RC time constants of coupling networks. This circuit has no stable state since internal switching circuits keep it oscillating between states. The trigger pulse is generated internally.

Bistable Multivibrator--Bistable multivibrators, called flip flops, switch from high to low or low to high under the control of an external switching pulse. This circuit has two stable states and can be switched from one state to the other only by applying a trigger pulse. Bistable multivibrators are used extensively in digital circuits and come with a variety of switching and control characteristics.

Monostable Multivibrator--A monostable multivibrator, called a one shot has only one stable state. When driven out of its stable state by a switching control pulse, it will return to its stable state due to internal switching action. The time required for the circuit to return to its stable state after being switched is determined by an RC coupling circuit.

Multivibrators have two active states which are complementary, that is, when one element is high the other must be low. It is possible to use either or both outputs if complementary or inverse functions are desired. The outputs are usually designated by Q and $\bar{Q}$. When output is high, Q is high, $\bar{Q}$ must be low and the MV is in the 1 state. When output $\bar{Q}$ is high, Q must be low and the MV is in the 0 state.

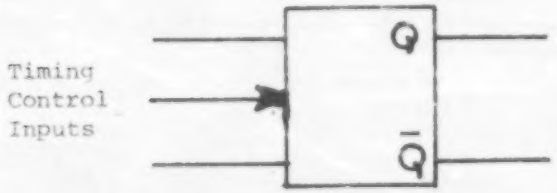


Figure 7.6 - Multivibrator Block Diagram

Pulse Shaping Circuits

Pulse shapes can be a critical factor in proper operation of switching circuits. Switching speeds, pulse amplitude and pulse duration are parameters which control noise, timing, and logic levels in digital circuits. A specific nomenclature is used to describe the defining parameters of pulse shapes. Figure 7.7 shows a square wave pulse and its shape defining parameters.

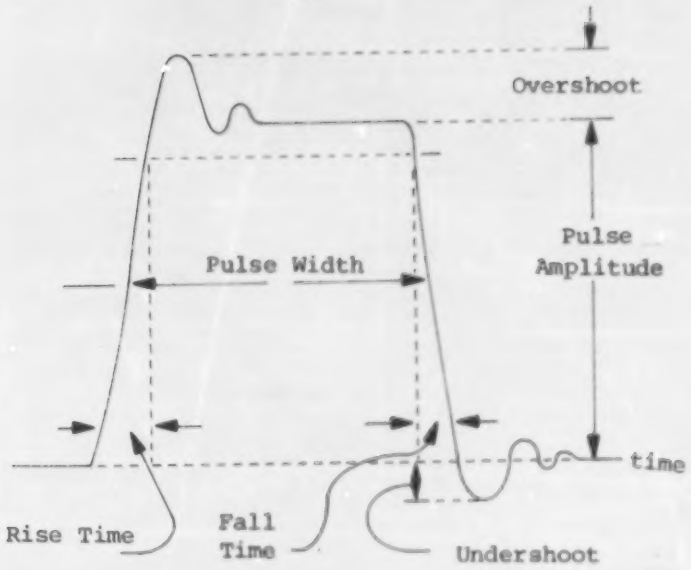


Fig. 7.7 SQUARE WAVE PULSE PARAMETERS

Special circuits are used to generate pulses with characteristics that fall within specified limits for proper circuit operations.

Schmitt Trigger

Pulse shaping circuits are used to quantify analog signals or to reshape digital pulses which have degenerated. One circuit used to perform pulse shaping is the schmitt trigger. A Schmitt trigger is a bistable multivibrator that is turned on and off by different levels of control signals. It has a very short rise and fall time when triggered. The voltage level which triggers the circuit from OFF to ON is called the upper trip point (UTP) and the voltage level which triggers it from ON to OFF is called the lower trip point (LTP). Output pulse duration time is the time required for the control signal to go from the UTP level to the LTP level. A small trigger symbol and a Schmitt trigger circuit with its trigger level and output are shown in Figure 7.8.

Schmitt Trigger IC Symbol

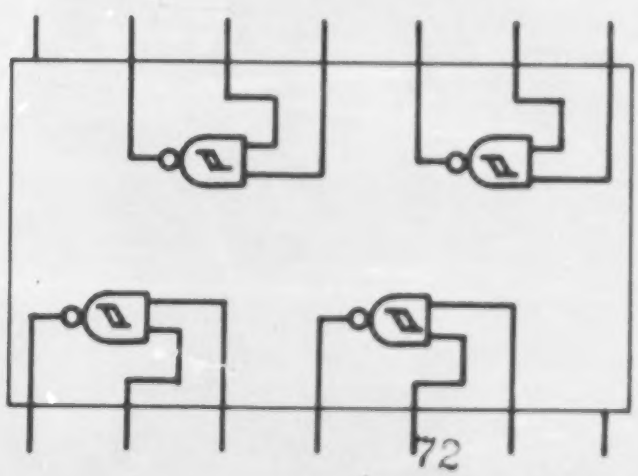


Fig. 7.8 (A)

Schmitt Trigger with Timing Diagram

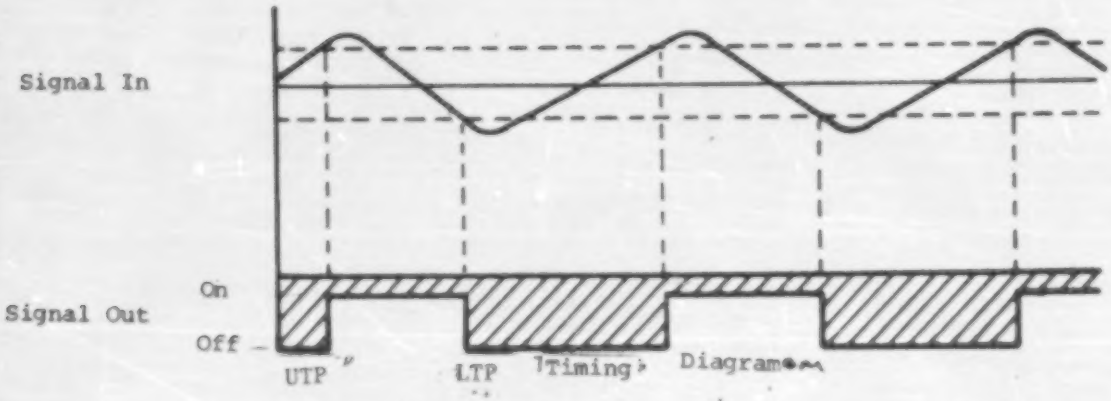


Fig. 7.8 (B)

Signal conditioning is essential to proper system performance even though the conditioning circuits are not part of the data control and manipulation

Differentiating networks and one shot multivibrators can also be used to produce pulses with rapid rise times and pulses of varying time durations.

Laboratory

Write the expression and construct a truth table for the following logic diagrams.

Verify the truth table using an OR gate and a NOR gate.

CHAPTER VIII

COMBINATIONAL LOGIC

Signal processing circuits which use various combinations of AND, OR, NAND, NOR and NOT gates are called combinational logic circuits.

Section A - Truth Tables

In the introduction to single gate operations a simple tabulation of all possible combinations of a two input gate was used. The output for each of these combinations was determined by the type of gate through which the signals were passed. The number of combinations possible in these tabulations depends upon the number of input variables used. For a single variable 'A' there are only two possible states, either A or $\bar{A}$ (NOT A). Since B can have two states, B and $\bar{B}$ (NOT B) and there can be two A states for each B, this makes a total of 4 different combinations of variable states. If 3 variables are used there are 8 possible combinations. If n variables are used there are 2^n possible combinations. A table of combinations for one, two and three variables is shown below.

ONE VARIABLE

A
0
1

TWO VARIABLES

A	B
0	0
0	1
1	0
1	1

THREE VARIABLES

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Possible Variable Combinations

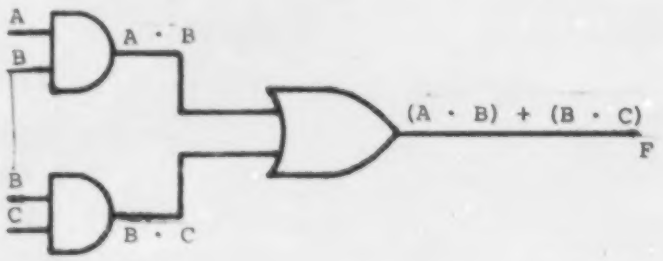
Section B - Circuit Synthesis and Analysis

Logic gates can be constructed to provide a specific output for any given combination of input variable states. The desired function can be written as a logic expression and from this expression an appropriate logic circuit can be constructed. Constructing a circuit for a given expression is the process of circuit synthesis. Deriving an expression for a given combination of logic gates is the process of circuit analysis.

Examples:

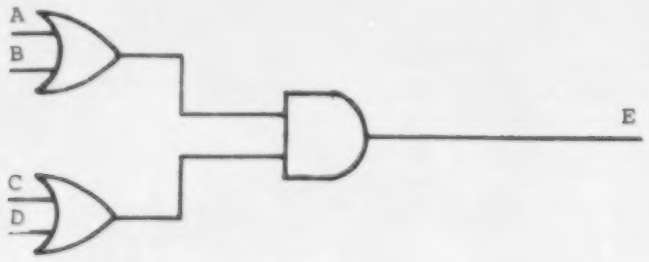
1. Determine the output of the following combinational logic circuit.

$F = (A \cdot B) + (B \cdot C)$



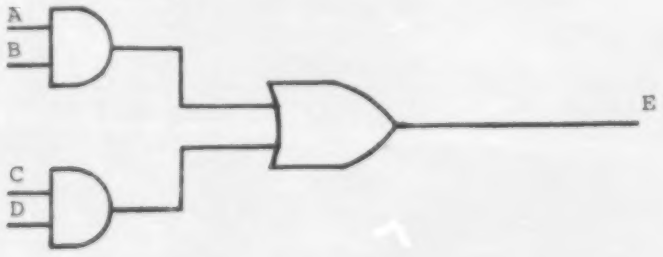
2. Construct a combinational logic circuit from the following expression.

$A + B \cdot C + D = E$



3. Write the expression for the following logic circuit.

$A \cdot B + C \cdot D = E$

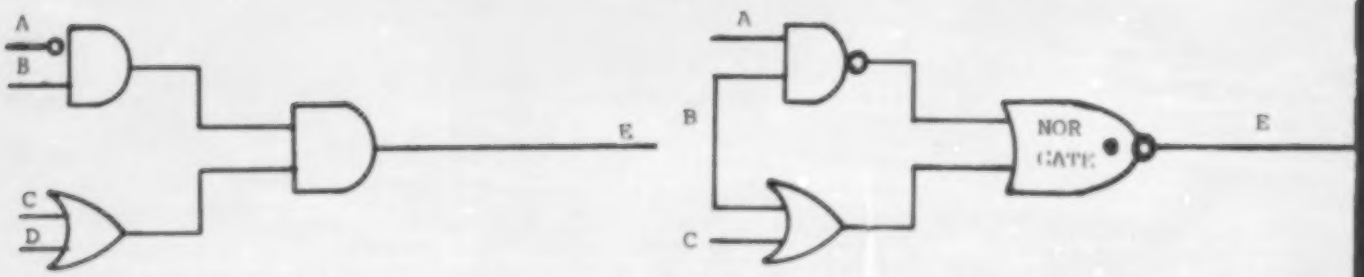


Exercises

1. Construct a logic diagram for each of the following logic expressions.

a) $A + \overline{B} \cdot B + \overline{C} = D$
b) $\overline{A \cdot B} + \overline{A} \cdot C = E$
c) $A \cdot B + C \cdot D + \overline{A} \cdot \overline{C} = F$

2. Write a logic expression for the output of each of the following circuits.



Logic Tables and Variable State Combinations

The logic function performed by AND, OR, and inverter gates produce either a 1 or 0 out depending on the logic level of the input variables. A table of AND, OR and invert logic functions is shown below.

Logical Multiplication (AND)	Invert (NOT)	Logical Addition (OR)
$0 \cdot 0 = 0$	$\overline{0} = 1$	$0 + 0 = 0$
$0 \cdot 1 = 0$	$\overline{1} = 0$	$0 + 1 = 1$
$1 \cdot 1 = 1$		$1 + 1 = 1$

Logic Function Table

The variable X can assume one of two states; it can be either 1 or 0, therefore we can say:

If $X = 1$, then $\overline{X} = 1 = 0$. and If $X = 0$, then $\overline{X} = \overline{0} = 1$.

also, $\overline{\overline{X}} = X$ also, $\overline{\overline{X}} = \overline{X}$

INVERT		AND	OR
X	$\overline{X}$	$X \cdot X = X$	$X + X = X$
0	1	$X \cdot \overline{X} = 0$	$X + \overline{X} = 1$
1	0	$1 \cdot X = 1$	$1 + X = 1$
		$0 \cdot X = 0$	$0 + X = X$

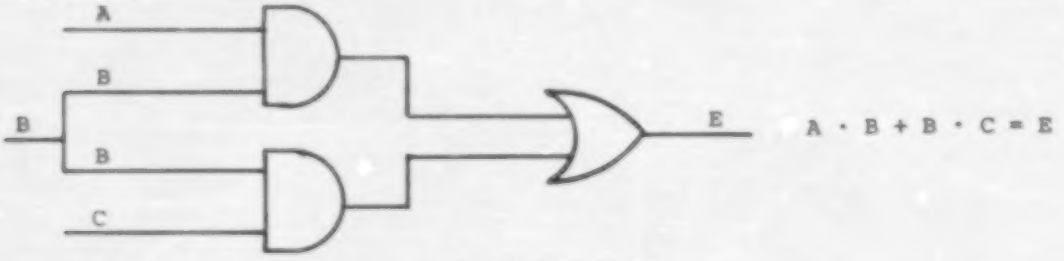
Variable State Combination Table

Combination A Logic Output

The output state of a combinational logic circuit can be determined by constructing a truth table for the logic expression and applying the rules of logical combinations established in the above logic table.

Example

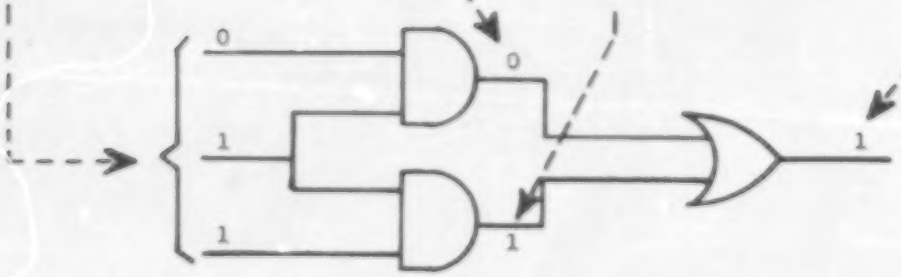
Determine the output state of the following logic circuit if A = 0, B = 1 and C = 1.



Logic Circuit

A	B	C	A · B	B · C	A · B + B · C
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	1	1	1

Truth Table



Logic Signal Diagram

Section C - Boolean Algebra

Synthesis of logic circuits is the process of developing a combination of large gates which will perform the function specified by a logic expression. In many cases the desired output can be achieved by several different choices of gate combinations. In cases where multiple variable combinations are used, some of the gate combinations may be redundant and therefore unnecessary. Designers should reduce the analytic expressions to their simplest terms to eliminate unnecessary circuity and optimize the final circuit configuration. The process of reducing circuit redundancy analytically is the subject of Boolean Algebra.

The relationships of logical combinations and the state relationships of variables can be combined to form a set of laws for Boolean Algebra. The validity of each law can be tested by allowing the variables in its expression to assume values of either 0 or 1 and show that the values on both sides of the equal sign are the same. Truth tables provide a method of keeping track of assigned values for variables in verifying the laws of Boolean Algebra. They can also be used as a direct means of simplifying a Boolean expression.

Laws of Boolean Algebra

The laws of Boolean Algebra are different from the laws of ordinary algebra. In Boolean Algebra, the same rules can be applied to logical product terms and logical sum terms. This is not true of ordinary algebraic relationships.

Distributive law: $A \cdot (B + C) = A \cdot B + A \cdot C$ (1)

$A + (B \cdot C) = (A + B) \cdot (A + C)$ (2)

Both of the above relationships are valid in Boolean Algebra, but only the first is a valid ordinary algebraic relationship.

The validity of Boolean expressions can be verified through the use of truth tables.

Example

Verify the above distributive law expressions using a truth table.

A	B	C	(B + C)	A·(B + C)	A·B	A·C	A·B + A·C
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

← Identical Results →

The truth table shows that A · (B + C) will produce the same outputs as A·B + A·C and verifies the distributive law:

$$A \cdot (B + C) = A \cdot B + A \cdot C$$

The second expression can be verified in a similar fashion.

A	B	C	(B · C)	A + (B · C)	A + B	A + C	(A + B)· (A + C)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

Identical Results

The above truth table proves the validity of the expression:

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

Example

Applications of the distributive law.

1. Prove:
   $A \cdot B + A \cdot \overline{B} = A$
   Proof:
   $A\,B + A\,\overline{B} = A \cdot (B + \overline{B})$ from 1 above

   $(B + \overline{B}) = 1$ from variable state combination tables

   $A \cdot (B + \overline{B}) = A \cdot 1 = A$

2. Prove:
   $(A + B) \cdot (A + \overline{B}) = A$
   Proof:
   $(A + B) \cdot (A + \overline{B}) = A + (B \cdot \overline{B})$ from 1 above

   $(B \cdot \overline{B}) = 0$ from variable state combination table

   $A + (B \cdot \overline{B}) = A + 0 = A$

Example

Simplify the following expression.

$$A \cdot B \cdot C + A \cdot B \cdot \overline{C} + A \cdot \overline{B}$$

Combine terms 1 and 2.

$$A \cdot B \cdot C + A \cdot B \cdot \overline{C} = A \cdot B \cdot (C + \overline{C}) = A \cdot B \cdot (1) = A \cdot B$$

Combine results above with term 3.

$$A \cdot B + A \cdot \overline{B} = A \cdot (B + \overline{B}) = A \cdot 1 = A$$

$$A \cdot B \cdot C + A \cdot B \cdot \overline{C} + A \cdot \overline{B} = A$$

Regardless of what values B and C assume, the output will always be the same as A, so the AND gates and OR gates are unnecessary.

The above results can be verified by use of a truth table.

Example

Reduce the following expression.

$$A \cdot \underset{①}{B} \cdot \overline{C} + A \cdot \underset{②}{\overline{B}} \cdot C + A \cdot \underset{③}{\overline{B}} \cdot \overline{C}$$

Combine terms 2 and 3.

④ $A \cdot \overline{B} \cdot C + A \cdot \overline{B} \cdot \overline{C} = A \cdot \overline{B} \cdot (C + \overline{C}) = A \cdot \overline{B} \cdot 1 = A \cdot \overline{B}$

Combine terms 1 and 3.

⑤ $A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} = A \cdot \overline{C} \cdot (B + \overline{B}) = A \cdot \overline{C} \cdot 1 = A \cdot \overline{C}$

Combining ④ and ⑤

$A \cdot \overline{B} + A \cdot \overline{C} = A \cdot (\overline{B} + \overline{C})$

$\therefore A \cdot B \cdot \overline{C} + A \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} = A \cdot \overline{B} + A \cdot \overline{C} = A \cdot (\overline{B} + \overline{C})$

From the above example it can be seen that a term may be used as often as needed in reducing combinations. This results from the fact that $X + X = X$ and $X \cdot X = X$ so that any term may be repeated in an expression as often as desired without changing the value of the expressions.

$$A\cdot B + A\cdot B + A\cdot B \cdot A\cdot B \cdot A\cdot B = A\cdot B$$

DeMorgan's Theorem

In a lab exercise for Chapter VII, expressions of DeMorgan's Theorem were developed. This theorem provides the basis for duality in Boolean expression. A general procedure for applying DeMorgan's Theorem to an expression is to change all AND symbols to OR'S, change all OR'S to AND'S and INVERT each term of the expression.

Examples

$$\overline{A + B} = \overline{A} \cdot \overline{B} \qquad \overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A \cdot B + \overline{B} \cdot C} = \overline{A} + \overline{B} \cdot B + \overline{C} \qquad A + \overline{B \cdot \overline{B} + C} = \overline{A}\,\overline{B} + B\,\overline{C}$$

Sum of Products--Product of Sums

Consider the expression: $A\cdot B\cdot\overline{C} + A\cdot\overline{B}\cdot C + \overline{A}\cdot B\cdot\overline{C} + A\cdot\overline{B}\cdot\overline{C} = F$ (Sum of Products)

The original terms in the left hand column of the above example are product terms. All variables in each term are ANDed or logically multiplied together forming a product. These terms are then ORed together or logically summed producing a total expression which is a SUM OF PRODUCTS. Sum terms which are logically ANDed form an expression which is a PRODUCT of SUMS.

A Boolean expression of terms set equal to '1' can be replaced with an inverted expression set equal to '0'. Either of these expressions may be used in the simplification process. They will produce combinations which differ only in the type of gate arrangement used to achieve the desired results. SUM of PRODUCT terms require AND gates feeding an OR gate. PRODUCT of SUMS terms requires OR gates feeding an AND gate. PRODUCT terms are called minterms and SUM terms are called maxterms.

Example

Simplify the following SUM of PRODUCTS expression above using min terms and maxterms.

TRUTH TABLE

A	B	C	F OUT	'0' Terms	'1' Terms
0	0	0	0	$\overline{A}\,\overline{B}\,\overline{C}$	
0	0	1	0	$\overline{A}\,\overline{B}\,C$	
0	1	0	1		$A\,B\,\overline{C}$
0	1	1	0	$\overline{A}\,B\,C$	
1	0	0	1		$A\,\overline{B}\,\overline{C}$
1	0	0	1		$A\,\overline{B}\,\overline{C}$
1	1	0	1		$A\,B\,\overline{C}$
1	1	1	0	$A\,B\,C$	

Grouping all of the terms which produce a '1' OUT form a Sum of Products expression.

$A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C}$ (Sum of Products)

Combine terms 1 and 3.

$$A \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} = B \cdot \overline{C}$$

Combine terms 2 and 4.

$$A \cdot \overline{B} \cdot C + A \cdot \overline{B} \cdot \overline{C} = A \cdot \overline{B}$$

$$A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} = A \cdot \overline{B} + B \cdot \overline{C} \text{ (minterms)}$$

Grouping all of the terms which produce a '0' OUT and applying DeMorgan's Theorum forms a Product of Sum Expression.

Write the expression for the product terms which produce 0 in the output column of the truth table and apply DeMorgan's Theorem to produce sum terms which equal 1. This is the maxterm equivalent of the original minterm expression.

$$\overline{\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,C} = \overline{0} = 1$$

$$(A + B + C) \cdot (A + B + \overline{C}) \cdot (A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C}) = 1 \quad \text{(Product of Sums)}$$

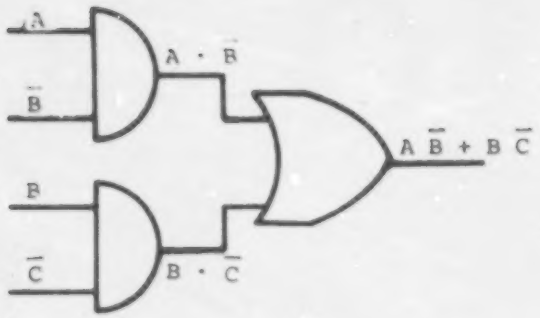
Combine terms 1 and 2.

$$(A + B + C)\ (A + B + \overline{C}) = (A + B)$$

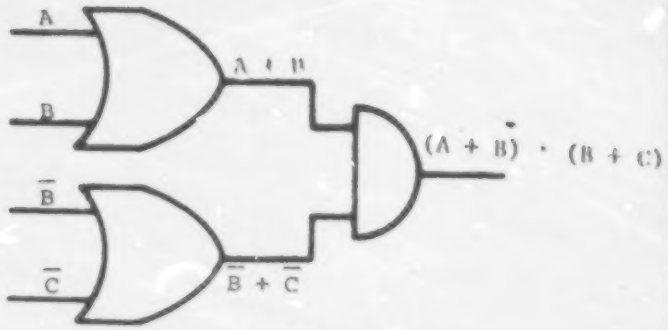
Combine terms 3 and 4.

$$(A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C}) = (\overline{B} + \overline{C})$$

$$A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} = (A + B) \cdot (\overline{B} + \overline{C}) \quad \text{(maxterm)}$$



Circuit to Implement Minterms



Circuit to Implement Maxterms

If the maxterm expression in the example above is expanded, it will produce a minterm expression identical to the reduced expression of the original minterm expression.

$$(A + B)\cdot(\overline{B} + \overline{C}) = A\cdot\overline{B} + B\cdot\overline{B} + B\cdot\overline{C} = A\cdot\overline{B} + B\cdot\overline{C}, \text{ (since } B\,\overline{B} = 0)$$

Karnaugh Mapping

Methods have been devised to facilitate the process of circuit simplification using Boolean Algebra. A widely used method of simplifying circuits of three and four variable expressions is Karnaugh Mapping. Since the simplification process is used primarily in circuit design, this introduction to Boolean Algebra will suffice for our present needs.

Problems

Write the maxterms for the following Boolean expressions.

$$F = A\cdot B\cdot C + A\cdot\overline{B}\cdot C + A\cdot B\cdot\overline{C}$$

$$F = \overline{A}\cdot\overline{B}\cdot C + A\cdot\overline{B}\cdot C + \overline{A}\cdot\overline{B}\cdot\overline{C}$$

Write the minterms for the following Boolean expressions.

$$F = (A + B + C)\cdot(\overline{A} + B + C)\cdot(A + B + \overline{C})$$

$$F = (\overline{A} + \overline{B} + \overline{C})\cdot(\overline{A} + B + \overline{C})\cdot(\overline{A} + B + C)$$

CHAPTER IX

BINARY ARITHMETIC

Section A - Binary Numbers

The Binary Number System is based on the use of only two symbols, 1 and 0. The Decimal Number System is based on the use of ten symbols, 0 through 9. In the Decimal system, a number larger than 9 must be represented by a combination of symbols. The position of the symbol relative to a decimal point determines the true value assigned to the symbol. The number 6. has a value of six; 60. has a value of 10 x 6 or sixty because the 6 is two places from the decimal point; 600. has a value of 100 x 6 or six hundred since the six is three places from the decimal point. The position of each digit relative to the decimal point determines the power of ten by which it must be multiplied to produce its true quantity. The decimal number 642 is equal to:

$$(10^2 \times 6)+(10^1 \times 4)+(10^0 \times 2)= \text{six hundred + forty + two}$$

Ten is the radix of the decimal system--it is the number by which digits in a number are multiplied to determine their positional value.

The weighted value of digits in any number system is determined by multiplying each digit by the system's radix raised to a power determined by its position relative to a radix point. For binary numbers the radix is 2 so each digit is multiplied by some power of 2 which increases to the left of the radix point and decreases to the right of the radix point (binary point).

$$101_2 = (2^2 \times 1)+(2^1 \times 0)+(2^0 \times 1)= 4 + 0 + 1 = 5$$

$$.101_2 = (1 \times 2^{-1})+(0 \times 2^{-2}) +(1 \times 2^{-3}) = 1/2 + 0 + 1/8 = 5/8$$

Example: Find the decimal values of the following binary numbers: 1010.011, 1101.101, 110.1

Position Values									Decimal Value
$2^N \cdots 2^3$	2^2	2^1	2^0	·	2^{-1}	2^{-2}	$2^{-3} \cdots 2^{-N}$		
1	0	1	0	·	0	1	1	⟶	10.375
1	1	0	1	·	1	0	1	⟶	13.625
0	1	1	0	·	1	0	0	⟶	6.5

To convert a decimal number to its binary equivalent, divide the decimal number by 2 and place in the binary number position a '0' if no remainder is obtained and a 1 if a remainder is obtained. The first value obtained is the least significant digit (LSD).

Example

Convert 25_{10} to its binary equivalent.

Division	Remainder	Binary Digit
		. Radix point
2 |25	R=1	1
2 |12	R=1	1
2 |6	R=0	0
2 |3	R=0	0
2 |1	R=1	1
0	R=1	1 ↑ READ UP

$$25_{10} = 11001_2$$

To convert the fractional part of a decimal number to binary, multiply the decimal number by two and place in the number position A '0' if a whole number is not generated and a '1' if a whole number is generated. Remove the whole number and continue multiplying the fractional number only.

Example

Find the binary equivalent of 0.36_{10}.

	Binary Digit
.36	. Radix point
2	
.72	0
2	
X.44	1
2	
.88	0
2	
X.76	1
2	
X.52	1
2	
X.04	1

$0.36_{10} = .010111_2$ etc.

Problems

Convert the following binary numbers to decimal values.

1011.110 1100.0101 10010.0110

Convert the following decimal numbers to binary. (Carry to 6 places after radix point.)

36.25 29.5 18.625

Arithmetic Circuits

Binary arithmetic can be performed by switching circuits in many ways. Circuits used and logic operations performed in implementing an arithmetic operation are a matter of choice of the system designer. A sequence of operational steps used to perform specific operations is called an algorithm. The choice of algorithms used to solve problems depends on both applications and economics. A simple algorithm for performing multiplication is to use repeated addition, $6 \times 4 = 6 + 6 + 6 + 6$. A simple algorithm for performing division is using repeated subtraction and counting the number of times the divisor has to be subtracted from the dividend to make the final difference 0 or as close to 0 as system limitations will permit. $18 \div 6$ can be determined by $18 - 6 - 6 - 6 = 0$ or 3 subtractions.

Binary Adders

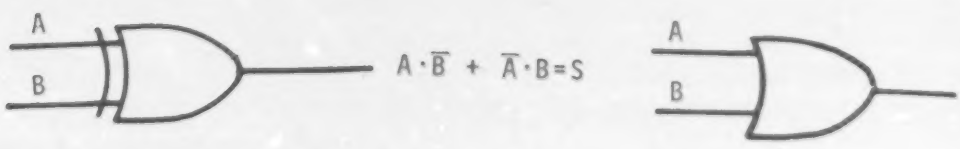
Consider the simplest addition that can be performed: the addition of only two digits. Construct a table of results for all possible combinations of two variables. A circuit which will perform the operation shown in the truth table is called a half adder.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

S = Sum
C = Carry

Half Adder Truth Table

The hardware needed to implement the operation shown is a combination of gates which will produce a '1' [illegible] for the following logic expressions $(A \cdot \overline{B}) + (\overline{A} \cdot B)$ and a '0' out for [illegible] others. This circuit is recognized from previous discussions as an EXCLUSIVE OR (XOR) circuit. An XOR circuit will produce the sum output for a half adder. A carry output is produced only when A and B are both 1. The carry output therefore requires only a simple AND gate.



Exclusive OR Gate

AND Gate

Figure 9.1

The addition of two numbers cannot be performed correctly by a half adder since no provision is made to accommodate the carry generated by adding 1 + 1. Another half adder is needed to add a carry digit.

Full Adder

A full adder consists of two half adders, one to add the addend and one to add the carry generated by addition of the two previous digits. A truth table for a full adder must include the additional variable Ci to determine the sum and carry out values that will be generated by the total addition process. A and B are the two numbers to be added and Ci is the 'Carry in' number generated by addition of the previous digits in the sequence.

IN			OUT	
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = \bar{A}\cdot\bar{B}\cdot C + \bar{A}\cdot B\cdot\bar{C} + A\cdot\bar{B}\cdot\bar{C} + A\cdot B\cdot C$$

$$Co = \bar{A}\cdot B\cdot C + A\cdot\bar{B}\cdot C + A\cdot B\cdot\bar{C} + A\cdot B\cdot C$$

which reduces to

$$Co = A\cdot B + B\cdot C + A\cdot C$$

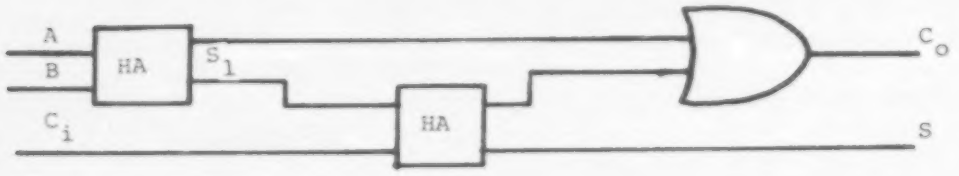


Figure 9.2 Truth Table & Block Diagram of Full Adder

Binary Subtractors

Half Subtractor

The process of binary subtraction can be implemented in much the same way as binary addition. From a truth table for subtraction of one digit from another a half subtractor can be defined. A half subtractor makes no provision for handling a borrow term resulting from the subtrahend digit being larger than the menuend digit. A truth table and circuit diagram for half subtractor X-Y is shown in Figure 9.3.

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D = Difference
B = Borrow
$D = X \cdot \bar{Y} + \bar{X} \cdot Y$
$B = X\,Y$

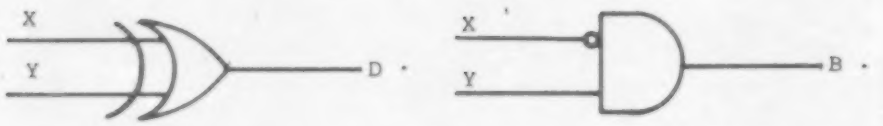


Figure 9.3 Truth Table and Logic Circuit for Half Subtractor

The second row of the truth table says that in order to subtract 1 from 0, a borrow from the next most significant digit must be made so a 1 is placed in the B column. The value of the menuend X is then increased by 2. When the new value of X is diminished by the value in Y, it leaves a difference of 1 as indicated in column D.

Full Subtractor

A full subtractor performs the borrow operation by subtracting 1 from the next MSD when required. An additional variable Bi (Borrow in) is included in the truth table to indicate the circuit combinations needed to implement this borrow operation. A truth table and circuit for a full subtractor is shown in Figure 9.4. Bi (Borrow in) means the minuend has been borrowed from in a previous operation. Bo (Borrow out) means the minuend must borrow from the next most significant digit (MSD).

Example

$$\begin{array}{r} 1\,0\,0\,1 \\ -\,0\,1\,1\,0 \\ \hline 0\,0\,1\,1 \end{array}$$

D = X - Y

IN			OUT	
X	Y	Bi	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = \bar{X}\cdot\bar{Y}\cdot Bi + \bar{X}\cdot Y\cdot\overline{Bi} + X\cdot\bar{Y}\cdot Bi + X\cdot Y\cdot Bi$$

$$Bo = \bar{X}\cdot\bar{Y}\cdot Bi + \bar{X}\cdot Y\cdot\overline{Bi} + \bar{X}\cdot Y\cdot Bi + X\cdot Y\cdot Bi$$

$$Bo = \bar{X}\cdot Bi + \bar{X}\cdot Y = Y\cdot Bi$$

Figure 9.4 Full Subtractor X - Y

Section B - Complemented Numbers

Decimal Complements

The process of subtraction may be performed by addition using complements of negative numbers. One of two types of complemented numbers may be used, either the true complement or the radix minus one complement. In the decimal system the radix minus one complement of a number is found by subtracting each digit of the number from 9. The true complement is found by adding one to the least significant digit of the radix minus one complement.

Example

Find the true complement and radix minus one complement of 697.45.

Radix minus one	999.99		
Subtract	697.45	Radix	1000.00
Radix minus one complement	302.54	Subtract	697.45
Add 1 to LSD	1	True Complement	302.55
True complement	302.55		

When performing subtraction by adding complemented negative numbers to noncomplemented positive numbers, a carry will be generated by addition of the most significant digits. Disregard the carry digit when true complements are used. Add the carry to the LSD of answer when radix minus one complement is used.

Example

Subtract 23 from 56 using true and radix minus one complements.

Step 1 - Find the true complement and radix minus one complement.

True complement of -23 = 77
Radix minus one complement of -23 = 76

Step 2 - Perfrom subtraction using the true complement.

56		56
-23	True Complement	+77
33	Drop the carry digit	133 = 33

Step 3 - Perform subtraction using the radix minus 1 complement.

56		56
-23	Radix minus one complement	76
33	End around carry	132
	Add carry to LSD	+ 1
		33

Binary Complements

The same procedure can be used to perform subtraction in the binary system. The radix minus one complement or 1's complement of a binary number is found by subtracting each digit from 1 which is the same as changing all 0's to 1's and all 1's to 0's. The true complement, or 2's complement is found by adding 1 to the least significant digit (LSD) of the 1's complement.

Example

Find the 1's and 2's complement of the following binary number.

Given binary number	10110.10
To find radix minus 1 complement	
(1's complement)	11111.11
Subtract	10110.10
1's complement	01001.01

Procedure for finding the radix minus 1 complement

To find the true complement (2's complement)

1's complement	01001.01
Add 1 to LSD	1
True complement	01001.10

Procedure for finding the true complement

The same rule for handling a carry generated by addition of MSD's as shown for decimal numbers applies to binary numbers. For 2's complement the carry is dropped. For 1's complement the carry is added to the LSD of the answer.

Example:

Subtract 101.01 from 11011.10 using straight subtraction, using 1's complements; using 2's complements.

NOTE: Always place as many digits in the subtrahend as are given in the menuend.

By subtraction		11011.10	27.5
		-00101.01	- 5.25
	Ans.	10110.01	22.25

1's complement of 00101.01 = 11010.10

2's complement of 00101.01.= 11010.11

1's complement		11011.10	2's complement	11011.10	
		11010.10		11010.11	
end around carry	1	10110.00	drop carry 1	10110.01	Ans.
		1			
Ans.		10110.01			

Exercise

Subtract 17_{10} from 66_{10} using binary numbers and both 1's and 2's complements.

ANS. 110001

SIGNED NUMBERS

The sign of binary numbers, + or -, is denoted by placing a 1 to the left of the numbers MSD for negative numbers and an 0 to the left of the MSD for positive numbers. In 1's and 2's complement system a 1 in the sign bit position means that the number which follows is in complemented form. In binary addition and subtraction using complement operation the sign bit is treated as another digit. In arithmetic operation the sign of the answer is generated by the summing process. If an answer has a 1 in its sign bit position, answer is negative, and the true magnitude of the answer is the complement of the number shown.

Example

Write the following numbers in binary using a sign bit.

+ 12 →0.1100
- 13 →1.1101
- 5 →1.0101
+ 10 →0.1010

Example

Write the above numbers as they would appear in a 1's complement system.

+ 12 →0.1100
- 13 →1.0010
- 5 →1.1010
+ 10 →0.1010

Example

Subtract 13 from 25 using a 1's complement binary system.

```
                + 25 →0.11001
                - 13 →1.10010  -  complement of 01101
end around carry    ↱1 10.01011
                    ↳      1
                + 12   0.01100
```

Example

Subtract 25 from 13 using 1's complements.

```
+ 13 → 0.01101
- 25 → 1.00110
```

Complement 1.10011 - Answer is a complemented negative number

Magnitude - 01100 = -12

Example

Add -25 and -13 using 1's complements. NOTE: Provide enough places to avoid overflow. 4

```
                -25   1.100110
                -13   1.110010
End around carry  1   1.011000
                  ↳         1
                      1.011001
Complement              - 100110  ⇒ -38
Magnitude
```

Examples

Complement subtraction - signed numbers.

1's complement

```
+ 10   + 1010  → 0.1010
- 12   - 1100  → 1.0011
                  1.1101   =  -0010₂
```

```
- 10   -01010  → 1.10101
- 12   -01100  → 1.10011
                 11.01000
End around carry ↳      1
                  1.01001  =  -10110₂
```

2's complement

```
+  7   + 0111  → 0.0111
-  9   - 1001  → 1.0111 ←  Two's complement
                  1.1110 =  -0010₂
```

```
- 14   -01110  → 1.10010 ←
-  6   -00110  → 1.11010 ←  Two's complement
Drop the carry →  1.01100 =  -10100₂
```

```
+ 15   + 1111 → 0.1111  ← Two's complement
-  8   - 1000 → 1.1000
Drop the carry → 1.0.0111  =  0.0111₂
```

Exercise

Perform the following arithmetic operation in binary using signed numbers in a 2's complement system.

12 + 15
28 - 14
-15 + 2
-33 - 8

Multiplication and Division

As mentioned earlier, the arithmetic operations of multiplication and division may be performed by repeated additions and subtractions. Other algorithms have been developed for performing multiplication and division with fewer operations. These algorithms make use of the fact that shifting a number left one place is the same as multiplying by its radix and shifting right divides the number by its radix. Multiplying by 0 produces a partial product of 0 and multplying by 1 produces partial product equal to the multiplicand. The simplicity of developing partial products and performing shifting operations makes the implementation of multiplication and division algorithms easy to achieve even though many operations may be required.

Lab Exercises: Construct a full adder from a given circuit diagram
Construct a full subtractor from a given circuit diagram
Perform subtraction using an adder and complemented numbers